VITESSE

VSC8221
Data Sheet

Single-Port 10/100/1000BASE-T PHY with 1.25 Gbps SerDes for SFPs/GBICs

1 General Description

Ideally suited for Ethernet Switches with SGMII/SerDes MAC Interfaces, Media Converter applications, and SFP/GBIC modules, the industry-leading, low-power VSC8221 from Vitesse integrates a high-performance 1.25Gbps SerDes and a triple speed (10/100/1000BASE-T) transceiver, providing unmatched tolerance to noise and cable plant imperfections.

Consuming approximately 700mW and eliminating the need for external power supply regulators, the device requires only a single 3.3V power supply. To further minimize system complexity and cost, the VSC8221's twisted pair interface features fully integrated line terminations, exceptionally low EMI, and robust Cable Sourced ESD (CESD) performance.

The VSC8221 offers direct connectivity to SGMII or SerDes interfaces. In 1000BASE-X SerDes mode, the VSC8221 may be used to connect a MAC to copper media (MAC to Cat-5) or to 100BASE-FX (over its copper media interface). In SGMII mode, the VSC8221 provides a fully compliant, 4-pin or 6-pin interface to MACs. The 1000BASE-X SerDes and SGMII interfaces offer either automatic or user-controlled auto-negotiation priority resolution between the 1000BASE-X and 1000BASE-T auto-negotiation processes. A single chip copper-to-optics Media Converter can be easily implemented by simultaneous use of the SerDes and Cat-5 media interfaces.

To minimize power consumption, the VSC8221 offers several programmable power management modes. The device also supports the comprehensive VeriPHY® Cable Diagnostics feature from Vitesse, offering the system manufacturer and IT administrator a complete suite of cable plant diagnostics to simplify the manufacture, installation, and management of Gigabit-over-copper networks.

2 Features and Benefits

Features	Benefits
• Very low power consumption	• Reduces power supply costs • Fully compliant with SFP MSA's power dissipation specification of less than 1W maximum per module
• Single 3.3V power supply with on-chip regulator	• Eliminates external regulators, reducing system costs
• SGMII & SerDes Interfaces	• Connects to serial MACs or optical modules • Supports triple-speed copper SFP/GBIC modules
• Patented line driver with integrated line side termination resistors	• May allow use of SimpliPHY'd Magnetics with up to 50% cost savings versus competition • Saves over 12 external components per port and reduces PCB area and cost by 50% • Can enable a superior, FCC Class B capable EMI solution for copper SFPs
• Over 150m of Cat-5 reach with the industry's highest noise tolerance	• Ensures trouble-free deployment in real world Ethernet networks
• Several flexible power management modes	• Reduces power consumption and system cost
• Small footprint 9mm x 9mm, 100-TFBGA package	• Suitable for Gigabit switch ports, SFPs/GBICs, and media converters

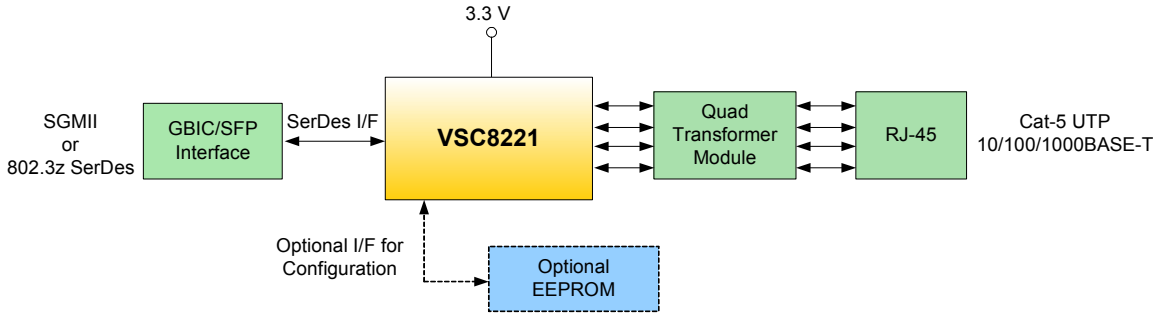
3 Applications

- Triple-speed SFP/GBIC modules
- Media converters

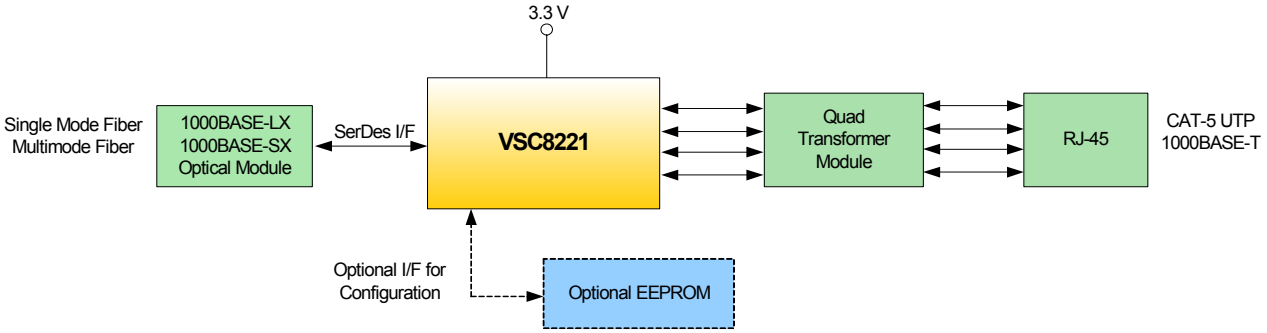
© *VITESSE SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896
Internet: www.vitesse.com

4 Applications Diagrams

4.1 SFP/GBIC Serial Interface (SGMII or 802.3z SerDes) to Cat-5



4.2 Media Converter (1000BASE-X to Cat-5)



5 Device Block Diagram

The diagram below depicts the primary functional blocks and pins for the VSC8221 IC.

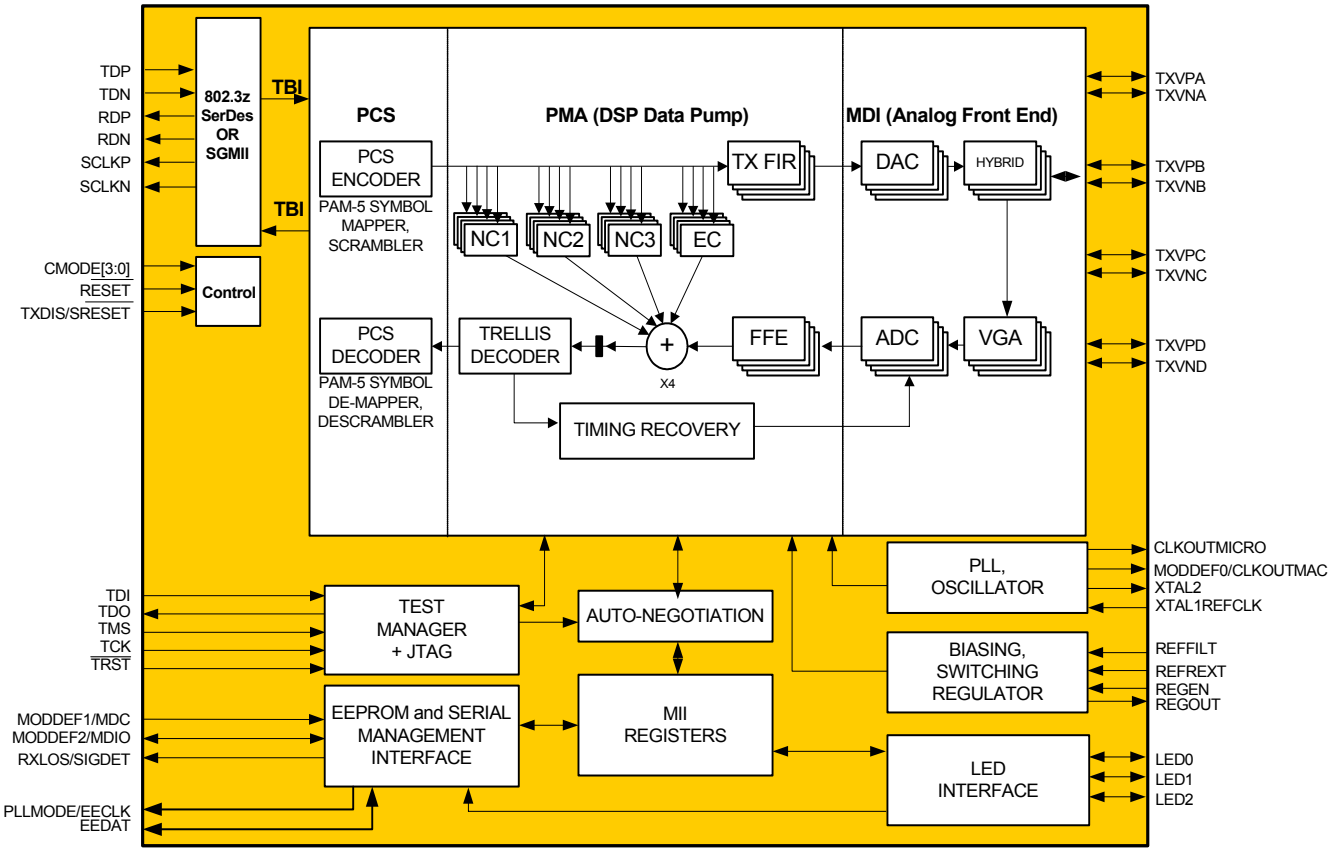


Figure 1. VSC8221 Block Diagram

6 Relevant Specifications & Documentation

The VSC8221 conforms to the following specifications. Please refer to these documents for additional information.

Table 1. Specifications and Documentation

Specification - Revision	Description
IEEE 802.3-2002	Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. IEEE 802.3-2002 consolidates and supersedes the following specifications: 802.3ab (1000BASE-T), 802.3z (1000BASE-X), 802.3u (Fast Ethernet), with references to ANSI X3T12 TP-PMD standard (ANSI X3.263 TP-PMD)
IEEE 1149.1-1990	Test Access Port and Boundary Scan Architecture[1]. Includes IEEE Standard 1149.1a-1993 and IEEE Standard 1149.1b-1994
JEDEC EIA/JESD8-5	2.5V±0.2V (Normal Range), and 1.8V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits
JEDEC JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) Revision of JESD22-A114-A
JEDEC JESD22-A115-A	Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) Revision of EIA/JESD22-A115
JEDEC EIA/JESD78	IC Latch-Up Test Standard
MIL-STD-883E	Miltary Test Method Standard for Microcircuits
Cisco SGMII v1.7	Cisco SGMII specification
PICMG 2.16	IP Backplane for CompactPCI
Advanced TCA™ Base PICMG 3.0	IP Backplane specification for CompactPCI v3.0
Cisco InLine Power Detection Algorithm	Cisco Systems InLine Power Detection: http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml
Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement	Specification for pluggable fiber optic transceivers. Describes module data access protocol and interface

[1] Often referred to as the “JTAG” test standard.

7 Data Sheet Conventions

Conventions used throughout this data sheet are specified in the following table.

Table 2. Data Sheet Conventions

Convention	Syntax	Examples	Description
Register number	RegisterNumber.Bit or RegisterNumber.BitRange	23.10 23.12:10	Register 23 (address 17h), bit 10 Register 23 (address 17h), bits 12, 11, and 10
Extended Page Register Number[1]	RegisterNumberE.Bit or RegiesterNumberE.BitRange	23E.10 23E.12:10	Extended Register 23 (address 17h), bit 10 Extended Register 23 (address 17h), bits 12, 11, and 10
Signal name (active high)	SIGNALNAME[2]	PLLMODE	Signal name for PLLMODE
Signal name (active low)	$\overline{\text{SIGNALNAME}}$[2]	$\overline{\text{RESET}}$	Active low reset signal
Signal bus name	BUSNAME[MSB:LSB][2]	RXD[4:2]	Receive Data bus, bits 4, 3, and 2

[1] For more information about MII Extended Page Registers, refer to Section 22: "PHY Register Set Conventions" on page 63.
[2] All signal names are in all CAPITAL LETTERS.

Contents

1 General Description 1

2 Features and Benefits 1

3 Applications 1

4 Applications Diagrams 2

4.1 SFP/GBIC Serial Interface (SGMII or 802.3z SerDes) to Cat-5 2
4.2 Media Converter (1000BASE-X to Cat-5) 2

5 Device Block Diagram 3

6 Relevant Specifications & Documentation 4

7 Data Sheet Conventions 5

8 Package Pin Assignments & Signal Descriptions 14

8.1 Package Ball Diagram 14
8.2 Ball Locations and Signal Names 15
8.3 Signal Type Descriptions 15
8.4 Detailed Pin Descriptions 16

9 System Schematics 27

9.1 System Schematic - SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode . 27
9.2 System Schematic - 100Mbps Fiber Media Implementation 28

10 Twisted Pair Interface 29

10.1 Twisted Pair Auto-Negotiation (IEEE802.3 Clause 28) 29
10.2 Twisted Pair Auto MDI/MDI-X Function 29
10.3 Auto MDI/MDI-X in Forced 10/100 Link Speeds 30
10.4 Forcing the PHY into MDI or MDI-X mode in 10/100/1000 Link Speeds 31
10.5 Twisted Pair Link Speed Downshift 31
10.6 100Mbps Fiber Support Over Copper Media Interface 31
10.6.1 Register Settings 31

11 Transformerless Operation for PICMG 2.16 and 3.0 IP-based Backplanes 32

12 Dual Mode Serial Management Interface (SMI) 33

12.1 PHY Register Access with SMI in MSA mode 33
12.1.1 Write Operation - Random Write 35
12.1.2 Write Operation - Sequential Write 36
12.1.3 Read Operation - Random Read 37
12.1.4 Read Operation - Sequential Read 38
12.2 PHY Register Access with SMI in IEEE Mode 38

12.3 SMI Interrupt 40

13 LED Interface 41

13.1 Serial LED Output 43

14 Test Mode Interface (JTAG) 44

14.1 Supported Instructions and Instruction Codes 45
14.2 Boundary-Scan Register Cell Order 46

15 Enhanced ActiPHY Power Management 47

15.1 Operation in Enhanced ActiPHY Mode 47
15.2 Low-Power State 48
15.3 LP Wake-Up State 48
15.4 Normal Operating State 48

16 Ethernet In-line Powered Device Support 49

16.1 Cisco In-Line Powered Device Detection Mode 49
16.2 In-Line Power Ethernet Switch Diagram 49
16.3 In-Line Powered Device Detection (Cisco Method) 50
16.4 IEEE 802.3af (DTE Power via MDI) 50

17 Advanced Test Modes 51

17.1 Ethernet Packet Generator (EPG) 51
17.2 CRC Counter 51
17.3 Far-End Loopback 51
17.4 Near-End Loopback 52
17.5 Connector Loopback 52

18 Hardware Configuration Using CMODE pins 53

18.1 Setting the CMODE Configuration Bits 53
18.2 CMODE Bit Descriptions 54
18.3 Procedure for Selecting CMODE Pin Pull-Up/Pull-Down Resistor Values 56

19 EEPROM Interface 57

19.1 Programming Multiple VSC8221s Using the Same EEPROM 57

20 PHY Startup and Initialization 61

21 PHY Operating Modes 62

22 PHY Register Set Conventions 63

22.1 PHY Register Set Structure 63
22.2 PHY Register Set Nomenclature 64
22.3 PHY Register Bit types 64

23 PHY Register Set 65

23.1 PHY Register Names and Addresses 65

23.2 MII Register Descriptions 67

23.2.1 Register 0 (00h) – Mode Control Register 67
23.2.2 Register 1 (01h) – Mode Status Register 69
23.2.3 Register 2 (02h) – PHY Identifier Register #1 70
23.2.4 Register 3 (03h) – PHY Identifier Register #2 71
23.2.5 Register 4 (04h) – Auto-Negotiation Advertisement Register 71
23.2.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register 72
23.2.7 Register 6 (06h) – Auto-Negotiation Expansion Register 73
23.2.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register 74
23.2.9 Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register 75
23.2.10 Register 9 (09h) – 1000BASE-T Control Register 76
23.2.11 Register 10 (0Ah) – 1000BASE-T Status Register #1 78
23.2.12 Register 11 (0Bh) – Reserved Register 79
23.2.13 Register 12 (0Ch) – Reserved Register 80
23.2.14 Register 13 (0Dh) – Reserved Register 80
23.2.15 Register 14 (0Eh) – Reserved Register 80
23.2.16 Register 15 (0Fh) – 1000BASE-T Status Register #2 80
23.2.17 Register 16 (10h) – Reserved 81
23.2.18 Register 17 (11h) – Reserved 81
23.2.19 Register 18 (12h) – Bypass Control Register 81
23.2.20 Register 19 (13h) – Reserved 83
23.2.21 Register 20 (14h) – Reserved 84
23.2.22 Register 21 (15h) – Reserved 84
23.2.23 Register 22 (16h) – Control & Status Register 84
23.2.24 Register 23 (17h) – PHY Control Register #1 86
23.2.25 Register 24 (18h) – PHY Control Register #2 87
23.2.26 Register 25 (19h) – Interrupt Mask Register 88
23.2.27 Register 26 (1Ah) – Interrupt Status Register 90
23.2.28 Register 27 (1Bh) – LED Control Register 92
23.2.29 Register 28 (1Ch) – Auxiliary Control and Status Register 94
23.2.30 Register 29 (1Dh) – Reserved 96
23.2.31 Register 30 (1Eh) - MAC Interface Clause 37 Auto-Negotiation Control and Status 96
23.2.32 Register 31 (1Fh) – Extended Page Access 98

23.3 Extended MII Registers 98

23.3.1 Register 16E (10h) - Reserved 98
23.3.2 Register 17E (11h) - Serdes Control Register 98
23.3.3 Register 18E (12h) - Reserved 99
23.3.4 Register 19E (13h) - SerDes Control # 2 99
23.3.5 Register 20E (14h) - Extended PHY Control Register #3 100
23.3.6 Register 21E (15h) - EEPROM Interface Status and Control Register 101
23.3.7 Register 22E (16h) - EEPROM Data Read/Write Register 102
23.3.8 Register 23E (17h) - Extended PHY Control Register #4 103
23.3.9 Register 24E (18h) - Reserved 103
23.3.10 Register 25E (19h) - Reserved 104

23.3.11 Register 26E (1Ah) - Reserved 104
23.3.12 Register 27E (1Bh) - Reserved 104
23.3.13 Register 28E (1Ch) - Reserved 104
23.3.14 Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1 105
23.3.15 Register 30E (1Eh) - 1000BASE-T Ethernet Packet Generator Register #2 106

24 Electrical Specifications 107

24.1 Absolute Maximum Ratings 107
24.2 Recommended Operating Conditions 107
24.3 Thermal Application Data 108
24.4 Package Thermal Specifications - 100 TFBGA 109
24.5 Current and Power Consumption Estimates 109

25 DC Specifications 114

25.1 Digital Pins (VDDIO = 3.3 V) 114
25.2 Digital Pins (VDDIO = 2.5 V) 114
25.3 LED Output Pins (LED[2:0]) 115

26 Clocking Specifications 116

26.1 Reference Clock Option 116
26.2 Crystal Option 116

27 SerDes Specifications 117

28 System Timing Specifications 118

28.1 JTAG Timing 118
28.2 SMI Timing 119
28.3 MDINT Timing 120
28.4 Serial LED_CLK and LED_DATA Timing 120
28.5 REFCLK Timing 121
28.6 CLKOUT and CLKOUTMICRO Timing 122
28.7 Reset Timing 123

29 Packaging Specifications 124

29.1 100-Ball 9 × 9mm TFBGA Mechanical Specification 124
29.2 Package Moisture Sensitivity 124

30 Ordering Information 125

30.1 Devices 125

31 Design Guidelines 126

31.1 Required PHY Register Write Sequence 126
31.2 Interoperability with Intel 82547EI Gigabit Ethernet MAC+PHY IC 126
31.3 SerDes Jitter 126
31.4 SGMII 100BASE-TX Corruption of Packets with Odd Preambles 127

31.5 SGMII 100BASE-TX Corruption of Packets with no ESDs 127
31.6 Software Reset Time 128
31.7 Reducing EMI 128
31.8 Clause 40 Auto MDI/MDI-X Interoperability Testing 129
31.9 10BASE-T HDX Issue with IXIA Test Suite 129
31.10 100BASE-FX Initialization Script 129

32 Product Support 133

32.1 Available Documents and Application Notes 133

33 Document History and Notices 134

Figures

Figure 1. VSC8221 Block Diagram ... 3
Figure 2. 100 Ball TFBGA Package Ball Diagram ... 14
Figure 3. Signal Type Descriptions ... 15
Figure 4. System Schematic - SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode ... 27
Figure 5. System Schematic - 100Mbps Fiber Media Implementation ... 28
Figure 6. Twisted Pair Interface ... 29
Figure 7. Data Validity [D] ... 34
Figure 8. Start [S] and Stop [T] Definition ... 34
Figure 9. Acknowledge (by Receiver) [A] ... 34
Figure 10. Acknowledge (by Host) [H] ... 34
Figure 11. No Acknowledge (by Host) [N] ... 35
Figure 12. MDIO Read Frame ... 39
Figure 13. MDIO Write Frame ... 40
Figure 14. Logical Representation of MDINT Pin ... 40
Figure 15. Test Access Port and Boundary Scan Architecture ... 44
Figure 16. Enhanced ActiPHY State Diagram ... 47
Figure 17. In-line Powered Ethernet Switch Diagram ... 49
Figure 18. Far-end Loopback Block Diagram ... 51
Figure 19. Near-end Loopback Block Diagram ... 52
Figure 20. Connector Loopback ... 52
Figure 21. EEPROM Interface Connections ... 58
Figure 22. PHY Startup and Initialization Sequence ... 61
Figure 23. Extended Page Register Diagram ... 63
Figure 24. JTAG Interface AC Timing ... 118
Figure 25. SMI AC Timing ... 119
Figure 26. LED_CLK and LED_DATA Output AC Timing ... 120
Figure 27. REFCLK AC Timing ... 121
Figure 28. CLKOUT AC Timing ... 122
Figure 29. CLKOUTMICRO AC Timing ... 122
Figure 30. RESET AC Timing ... 123
Figure 31. 100-Ball 9 × 9mm TFBGA Mechanical Specification ... 124
Figure 32. SGMII Rx Path from the PHY to the MAC ... 127

Tables

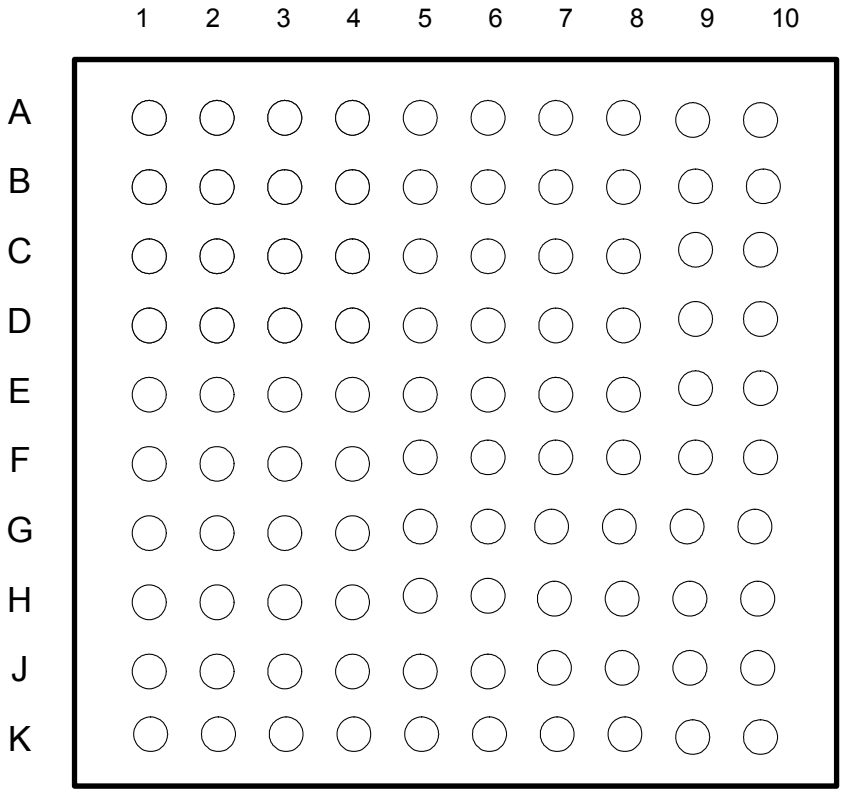
Table 1. Specifications and Documentation 4
Table 2. Data Sheet Conventions 5
Table 3. Signal Type Descriptions 15
Table 4. Configuration and Control Signals 16
Table 5. System Clock Interface Signals (SCI) 17
Table 6. Regulator Control and Analog Bias Signals 18
Table 7. JTAG Access Port 19
Table 8. Serial Management Interface Signals 20
Table 9. EEPROM Interface Signals 21
Table 10. LED Interface Signals 22
Table 11. Serial MAC Interface Signals 22
Table 12. Twisted Pair Interface Signals 24
Table 13. Power Supply and Ground Connections 25
Table 14. No Connects 25
Table 15. Power Supply and Associated Functional Signals 26
Table 16. MDI Wiring Pair Combinations 30
Table 17. SMI Pin Descriptions - MSA Mode 33
Table 18. SMI Pin Descriptions - IEEE Mode 38
Table 19. SMI Frame Format 39
Table 20. LED Function Assignments 41
Table 21. Parallel LED Functions 41
Table 22. LED Output Options 43
Table 23. JTAG Device Identification Register Description 44
Table 24. JTAG Interface Instruction Codes 45
Table 25. CMODE Pull-up/Pull-down Resistor Values 53
Table 26. CMODE Bit to PHY Operating Condition Parameter Mapping 54
Table 27. PHY Operating Condition Parameter Description 54
Table 28. Configuration EEPROM Data Format 58
Table 29. PHY Operating Modes 62
Table 30. Register Set Nomenclature 64
Table 31. PHY Register Bit Types 64

Table 32. PHY Register Names and Addresses 65
Table 33. PHY Operating Modes 86
Table 34. Absolute Maximum Ratings 107
Table 35. Recommended Operating Conditions 107
Table 36. Thermal Application Data 108
Table 37. Thermal Resistances 108
Table 38. Thermal Specifications - 100-Ball TFBGA 9 × 9mm package 109
Table 39. VDDIO at 3.3 V, SerDes-Cat-5, SCLK Disabled 109
Table 40. VDDIO at 3.3 V, SGMII-Cat-5 (1000 Mbps), SCLK Disabled 110
Table 41. VDDIO at 3.3 V, SGMII-Cat-5 (100 Mbps), SCLK Disabled 110
Table 42. VDDIO at 3.3 V, SGMII-Cat-5 (10 Mbps), SCLK Disabled 111
Table 43. VDDIO at 3.3 V SerDes-Cat-5, SCLK Enabled 111
Table 44. VDDIO at 3.3 V SerDes-Cat-5, SFP Mode On 112
Table 45. VDDIO at 3.3V SGMII-100BASE-FX, SFP Mode Off 112
Table 46. VDDIO at 3.3 V SerDes-Cat-5, SFP Mode On, Regulator On 112
Table 47. Digital Pins Specifications (VDDIO = 3.3 V) 114
Table 48. Digital Pins Specifications (VDDIO = 2.5 V) 114
Table 49. LED Output Pins Specification 115
Table 50. Reference Clock Option Specifications 116
Table 51. Crystal Option Specifications 116
Table 52. SerDes Specifications 117
Table 53. JTAG Timing Specifications 118
Table 54. SMI Timing Specifications 119
Table 55. MDINT Timing Specifications 120
Table 56. Serial LED_CLK and LED_DATA Timing Specifications 120
Table 57. REFCLK Timing Specifications 121
Table 58. CLKOUT and CLKOUTMICRO Timing Specifications 122
Table 59. RESET AC Timing Specification 123
Table 60. Part Number for the VSC8221 125
Table 61. Software Reset Times 128

8 Package Pin Assignments & Signal Descriptions

8.1 Package Ball Diagram

The following package ball diagram shows the view from the top of the package with the underlying BGA ball positions superimposed:



0.8 mm Ball Pitch (9 x 9 mm body size)
(Top View)

Figure 2. 100 Ball TFBGA Package Ball Diagram

8.2 Ball Locations and Signal Names

	1	2	3	4	5	6	7	8	9	10	
A	MODDEF0/ CLKOUT	$\overline{\text{RESET}}$	LED1	LED2	CMODE0	TXVPD	TXVPC	TXVPB	TXVPA	XTAL2	A
B	RXLOS/ SIGDET	TDO	LED0	CMODE3	CMODE1	TXVND	TXVNC	TXVNB	TXVNA	XTAL1/ REFCLK	B
C	NC	TCK	TDI	VDDIO-CTRL	CMODE2	VSS	VSS	VDD33A	VDDREG	REGEN	C
D	NC	NC	TMS	VSS	VSS	VSS	VSS	VSS	VDD33A	REGOUT	D
E	NC	NC	$\overline{\text{TRST}}$	VSS	VSS	VSS	VSS	VSS	VDD12A	REFREXT	E
F	NC	NC	VDD12	VSS	VSS	VSS	VSS	VDD12	EECLK/ PLLMODE	REFFILT	F
G	NC	NC	VDD12	VSS	VSS	VSS	VSS	$\overline{\text{TXDIS}}$/ $\overline{\text{SRESET}}$	EEDAT	VDD12	G
H	NC	NC	NC	VDDIO	NC	VSS	VDD12	VDDIOMI-CRO	MDINT	CLKOUTMI-CRO/$\overline{\text{OSC-DIS}}$	H
J	NC	NC	NC	NC	NC	NC	SCLKP	SCLKN	MODDEF2/ MDIO	MODDEF1/ MDC	J
K	NC	NC	NC	NC	NC	NC	RDN	RDP	TDP	TDN	
	1	2	3	4	5	6	7	8	9	10	

Figure 3. Signal Type Descriptions

8.3 Signal Type Descriptions

Table 3. Signal Type Descriptions

Symbol	Signal Type	Description
I	Digital Input	Standard digital input signal. No internal pull-up or pull-down.
I_{PU}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100k pull-up to VDDIO, VDDIOMICRO,VDDIOCTRL or the VDD33A supply. Refer to Section 15: "Power Supply and Associated Functional Signals" for details.
I_{PU5V}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100k pull-up to VDDIO,VDDIOMICRO,VDDIOCTRL or the TXVDD supply. Refer to Section 15: "Power Supply and Associated Functional Signals" for details. This input pin is 5v tolerant.
I_{PD}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100k pull-down to GND.
I_{PD5V}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100k pull-down to GND. This input pin is 5V tolerant.
I_{DIFF}	Differential Input Pair	SerDes differential input pair with 100Ω or 150Ω differential terminations. Pins should be AC-coupled with external 0.01µF capacitors.

Table 3. Signal Type Descriptions *(continued)*

Symbol	Signal Type	Description
O	Digital Output	Standard digital output signal.
O_{ZC}	Impedance Controlled Output	50Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive, 125MHz clock output pins, in addition to high speed manufacturing test mode pins.
O_{DIFF}	Differential Output Pair	SerDes differential output pair, with on-chip 100Ω or 150Ω differential terminations. Pins should be AC-coupled with external 0.01µF capacitors.
I/O	Digital Bidirectional	Tristate-able, digital input and output signal.
I_{PU}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100k pull-up to VDDIO,VDDIOMICRO,VDDIOCTRL or the VDD33A supply. Refer to Section 15: "Power Supply and Associated Functional Signals" for details.
I_{PD}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100k pull-down to GND.
OD	Digital Open Drain Output	Open drain digital output signal. Must be pulled to VDDIOMICRO through an external pull-up resistor.
A_{DIFF}	Analog Differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog Bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network, as shown in Section 9: "System Schematics".
I_A	Analog Input	Analog input for sensing variable voltage levels.
OS	Open Source	Open source digital output signal. Must be pulled to GND through an external pull-down resistor.
P	Power Supply	Power supply connection. Must be connected to specified power supply plane.
G	GND	Ground Connection. Must be connected to ground.
NC	No Connect	No connect signal. Must be left floating.

8.4 Detailed Pin Descriptions

Table 4. Configuration and Control Signals

100 TFBGA Ball	Signal Name	Type	Description
B4,C5,B5,A5	CMODE3 CMODE2 CMODE1 CMODE0	I_A	**Hardware Chip Mode Select.** The CMODE inputs are used for hardware configuration of the various operating modes of the PHY. Each pin has multiple settings, each of which is established by an external 1% resistor tied to GND or VDD33A. See "Hardware Configuration Using CMODE pins," page 53 for details on configuring the PHY with the CMODE pins.
A2	$\overline{\text{RESET}}$	I	**Hardware Chip Reset.** $\overline{\text{RESET}}$ is an active low input. When asserted, it powers down all of the internal reference voltages and the PLLs. It resets all internal logic, including the DSPs and the MII Management Registers. Hardware reset is distinct from soft reset which only resets the port to accept new configuration based on register settings.

Table 4. Configuration and Control Signals *(continued)*

100 TFBGA Ball	Signal Name	Type	Description
G8	TXDIS/ $\overline{\text{SRESET}}$	I_{PU}	**Transmit Disable or Software Reset.** When asserted, it places the PHY in a low power state, which includes disabling the SerDes interface. Although the device is powered down, non-volatile Serial Management Interface registers retain their values. TXDIS and $\overline{\text{SRESET}}$ are simply two names for the same function. The assertion state (active high or low respectively) of this input pin is determined by the value of MII Register 21E.15 'SFP MODE' set at startup using Hardware Configuration or using the EEPROM interface. Refer to "Hardware Configuration Using CMODE pins," page 53 and "EEPROM Interface," page 57 for details on configuration at startup.

Table 5. System Clock Interface Signals (SCI)

100 TFBGA BALL	Signal Name	Type	Description
B10	XTAL1/ REFCLK	I	**XTAL1 - Crystal Oscillator Input.** Enabled by pulling $\overline{\text{OSCDIS}}$ (Internal Oscillator Disabled) high, a 25MHz parallel resonant crystal, with a +/- 50ppm frequency tolerance, should be connected across XTAL1 and XTAL2. 33pf capacitors should be connected from XTAL1 and XTAL2 to ground when using AT cut-type crystal rated for a parallel capacitance of 20pf. PLLMODE should be left floating (or pulled low) on reset when a 25MHz crystal is used. **REFCLK - PHY Reference Clock Input.** The reference input clock can either be a 25MHz (PLLMODE is low) or 125MHz (PLLMODE is high) reference clock, with a +/-100ppm frequency tolerance. See EECLK / PLLMODE pin description for more details.
A10	XTAL2	O	**Crystal Output.** 25MHz parallel resonant crystal oscillator output. 33pF capacitors should be connected from both XTAL1 and XTAL2 to ground when using AT cut-type crystal rated for a parallel capacitance of 20pf. PLLMODE should be left floating (or tied low) on reset when using the 25MHz crystal. This output can be left floating if driving XTAL1/REFCLK with a reference clock.
H10	CLKOUTMI-CRO/ $\overline{\text{OSCDIS}}$	I_{PU}/O	**CLKOUTMICRO - Clock Output.** This is a 4MHz (default) or a 125MHz output clock depending on the value of MII Register 20E.8. The voltage levels of the clock are based on the VDDIOMICRO power supply. **$\overline{\text{OSCDIS}}$ - Active Low on-chip Oscillator Disable Input.** This input is sampled during the device power-up sequence or on assertion of $\overline{\text{RESET}}$. When sampled high, the PHY enables the internal on-chip oscillator allowing operation with a 25MHz crystal. When sampled low, the PHY's oscillator is turned off and the PHY must be supplied with an external 25MHz or 125MHz clock on the REFCLK pin.

Table 5. System Clock Interface Signals (SCI) *(continued)*

100 TFBGA BALL	Signal Name	Type	Description
A1	MODDEF0/ CLKOUT	O	The functionality of this signal pin depends on the value for MII Register 21E.15 'SFP Mode' which is set at startup. Refer to "Hardware Configuration Using CMODE pins," page 53, and "EEPROM Interface," page 57 for details on configuration at startup. **MODDEF0 – Active Low PHY Ready Indicator Output (valid in SFP Mode, when MII Register 21E.15 = 1).** This output is driven high immediately on PHY power-up or reset. This signal is asserted low after the PHY startup sequence has completed and the PHY has enabled access to the EEPROM connected to the EEPROM Interface through the Serial Management Interface. The minimum time this signal is high before being driven low is 10ms. The maximum time depends on the startup information stored in the EEPROM. Refer to "PHY Startup and Initialization," page 61 and "EEPROM Interface," page 57 for details. **CLKOUT – 125MHz Clock Output** (valid in IEEE Mode, when MII Register 21E.15 = 0). The PHY drives a 125MHz clock output after the PHY startup sequence has completed. This clock can be disabled by clearing MII Register 18.0. The voltage levels of this clock are determined by the VDDIO power supply.

Table 6. Regulator Control and Analog Bias Signals

100 TFBGA BALL	Signal Name	Type	Description
E10	REFREXT	A_{BIAS}	**REFREXT - Reference External Resistor.** Bias pin connects through external 2kΩ (1%) resistor to analog ground.
F10	REFFILT	A_{BIAS}	**REFFILT - Reference Filter.** Filter internal reference through external 0.1µF (10%) capacitor to analog ground.
C10	REGEN	A_{BIAS}	**REGEN- Regulator Enable.** Tie to VDD33A (3.3v) to enable the internal 1.2v regulator for normal chip operation.
D10	REGOUT	A_{BIAS}	**REGOUT - Regulator Supply Output.** This is the output of the on-chip switching regulator, which generates the primary 1.2v power supply voltage VDD12. REGOUT must be connected to an off-chip "LC" filter. See Section 9: "System Schematics" for more information.

Table 7. JTAG Access Port

100 TFBGA BALL	Signal Name	Type	Description
C3	TDI	I_{PU5V}	**JTAG Test Data Serial Input Data.** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
B2	TDO	O_{ZC}	**JTAG Test Data Serial Output Data.** Serial test data from the PHY is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
D3	TMS	I_{PU5V}	**JTAG Test Mode Select.** This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
C2	TCK	I_{PU5V}	**JTAG Test Clock.** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be pulled down with a 2kΩ pull-down resistor in designs that require JTAG functionality. This pin should be tied low in designs that do not require JTAG functionality.
E3	$\overline{TRST}$	I_{PU5V}	**JTAG Reset.** This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up (to VDDIOCTRL) resistor. Because of the internal pull-up, if the JTAG controller on the printed circuit board does *not* utilize the $\overline{TRST}$ signal, then the device will still function correctly when the $\overline{TRST}$ pin is left unconnected on the board. If the JTAG port of the PHY is not used on the printed circuit board, then this pin should be pulled down with a 2kΩ pull-down resistor or a falling edge must be provided to this pin after PHY power up.

Table 8. Serial Management Interface Signals

100 TFBGA BALL	Signal Name	Type	Description
J10	MODDEF1/ MDC	I	The Functionality of this pin is determined by the value of MII Register 21E.15 'SFP MODE' set at startup using CMODE Hardware Configuration or via the EEPROM interface. **MODDEF1 - Serial MSA Clock (valid in SFP Mode, when MII Register 21E.15 = 1).** MODDEF1 is the clock input of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the protocol specified in the MSA specification. Although typically operated at 100kHz, MODDEF1 can be operated at a maximum of 1MHz. **MDC - Management Data Clock (valid in IEEE Mode, when MII Register 21E.15 = 0).** MDC is the clock input of the two wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. Although typically operated at less than 100kHz due to frequency limitations of the EEPROM used with the PHY, the PHY registers can be accessed at a maximum frequency of 1MHz.
J9	MODDEF2/ MDIO	I/O	The Functionality of this pin is determined by the value of MII Register 21E.15 'SFP MODE' set at startup using CMODE Hardware Configuration or via the EEPROM interface. **MODDEF2 - Serial I/O Data (valid in SFP Mode, when MII Register 21E.15 = 1).** MODDEF2 is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the protocol specified in the MSA specification. This pin normally requires a 1.5kΩ to 4.7kΩ pull-up resistor to VDDIOMICRO at the Station Manager. The value of the pull-up resistor depends on the MODDEF1 frequency and the capacitive load on the MODDEF2 line. **MDIO - Serial I/OP Data (valid in IEEE Mode, when MII Register 21E.15 = 0)**. MDIO is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM Interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. This pin normally requires a 1.5kΩ to 4.7kΩ pull-up resistor to VDDIOMICRO at the Station Manager. The value of the pull-up resistor depends on the MDC frequency and the capacitive load on the MDIO line.

Table 8. Serial Management Interface Signals *(continued)*

100 TFBGA BALL	Signal Name	Type	Description
H9	$\overline{\text{MDINT}}$	OD	**Management Data Interrupt** $\overline{\text{MDINT}}$ is asserted whenever there is a change in the operating status of the device. This open drain signal indicates a change in the PHY's link operating conditions for which a Station Manager must interrogate to determine further information. See MII Register 25 and MII Register 26 for more information. The assertion polarity of $\overline{\text{MDINT}}$ is determined by the presence of a pull-up or pulldown on the $\overline{\text{MDINT}}$ pin. If the $\overline{\text{MDINT}}$ pin is pulled up to VDDIOMICRO using a 4.7kΩ τo 10kΩ resistor, it becomes an active low signal. If the $\overline{\text{MDINT}}$ pin is pulled down using a 4.7kΩ τo 10kΩ resistor, then it becomes an active high signal.

Table 9. EEPROM Interface Signals

100 TFBGA BALL	Signal Name	Type	Description
F9	EECLK/ PLLMODE	O_{ZC}/I_{PD}	**EECLK - EEPROM Clock Output.** This output is the clock line of the two-wire, MSA compliant, serial EEPROM Interface. This pin should be connected to the SCL input pin of the AT24 series of Atmel EEPROMs. Refer to "EEPROM Interface," page 57 for details. **PLLMODE - PLL Mode Select Input.** PLLMODE is sampled during the device power-up sequence or on reset. When PLLMODE is high, the PHY expects a 125MHz clock input as the PHY's reference clock. When low (default), a reference clock of 25MHz is expected at the REFCLK pin from either an external crystal or a clock reference. This pin is internally pulled down with a 100kΩ resistor.
G9	EEDAT	O_{ZC}/I_{PD}	**EEPROM Serial I/O Data.** This bidirectional signal is the data line of the two wire, MSA compliant, serial EEPROM Interface. This pin should be connected to the SDA pin of the AT24 series of Atmel EEPROMs. Refer to "EEPROM Interface," page 57 for details. The PHY determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when $\overline{\text{RESET}}$ is de-asserted. If EEDAT has a 4.7kΩ - 10kΩ external pull-up (to VDDIOMICRO) resistor, it assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.

Table 10. LED Interface Signals

100 TFBGA BALL	Signal Name	Type	Description
A4,A3,B3	LED2 LED1 LED0	O_{ZC}	**LED - Direct-Drive LED Outputs.** After reset, these pins serve as the direct drive, low EMI, LED driver output pins. All LEDs pins are active-low and driven at a 3.3V logic-high through the VDD33A analog power supply. The function of each LED can be set using hardware configuration or via MII Register 27. Refer "Hardware Configuration Using CMODE pins," page 53 and MII Register 27 for details.

Table 11. Serial MAC Interface Signals

100 TFBGA BALL	Signal Name	Type	Description
K9,K10	TDP TDN	I_{DIFF}	**Transmitter Data Differential Input Pair.** Differential 1.25Gbaud receiver inputs with register selectable on-chip 100Ω or 150Ω differential termination. The TDP and TDN signals should be AC-coupled with external 0.01µF series capacitors. See Section 9: "System Schematics" for further information.
K8,K7	RDP RDN	O_{DIFF}	**Receiver Data Differential Output Pair.** Differential 1.25 Gbaud transmitter outputs. External 0.01µF AC coupling capacitors should be located on the PHY side. The register selectable 100Ω or 150Ω differential termination should be placed near the MAC side. For more information, see Section 9.1, "System Schematic - SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode" on page 9-27. For more information on adjusting the output swing of these pins, see "Register 17E (11h) - Serdes Control Register," page 98.
J7,J8	SCLKP SCLKN	O_{DIFF}	**SGMII Clock Differential Output Pair.** This signal pair is a differential 625MHz SGMII clock for the SGMII data in accordance with Cisco's SGMII specification. These pins should be AC-coupled with external 0.01µF series capacitors or left unconnected when not used. For more information, see Section 9.1, "System Schematic - SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode" on page 9-27. For more information on adjusting the output swing of these pins, see "Register 17E (11h) - Serdes Control Register," page 98.

Table 11. Serial MAC Interface Signals *(continued)*

100 TFBGA BALL	Signal Name	Type	Description
B1	RXLOS/ SIGDET	I/O	The functionality of this signal pin depends on the value of MII Register 21E.15 'SFP Mode' which is set at startup. Refer to "Hardware Configuration Using CMODE pins," page 53 and "EEPROM Interface," page 57 for details on configuration at startup. **RXLOS - Receiver Loss of Signal Output (valid in SFP Mode, when MII Register 21E.15 = 1).** This active high signal is asserted when the Cat-5 link goes down. The pulse width of the RXLOS signal is configurable. Refer to MII Register 30.1:0 for details. **SIGDET - SerDes Signal Detect (I/O) (valid in IEEE Mode, when MII Register 21E.15 = 0).** SIGDET can be configured as an input or output and can be configured to function as active low or active high at startup using hardware configuration or the EEPROM interface. Refer to "Hardware Configuration Using CMODE pins," page 53 or "EEPROM Interface," page 57 for details on configuration at startup. SIGDET as Input: When used as an input, the SIGDET signal is meant to be connected to the signal detect output of the fiber optic transceiver. If SIGDET is high, this indicates receive activity on the fiber optic transceiver. If SIGDET is not used as an input, the PHY internally generates the signal detect function, from the incoming data on the TDP and TDN signal pins. SIGDET as Output: For Serial MAC to CAT5 Media PHY Operating modes, SIGDET is asserted if a valid CAT5 link has been established.

Table 12. Twisted Pair Interface Signals

100 TFBGA BALL	Signal Name	Type	Description
A9	TXVPA	A_{DIFF}	**TX/RX Channel "A" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "A" data channel. In all three speeds, this signal generates the secondary side signal, normally connected to RJ-45 pin 1. In 100BASE-FX mode, it is connected instead to the positive SFP transmit data signal (SFP_TD+). See Section 9: "System Schematics" for details.
B9	TXVNA	A_{DIFF}	**TX/RX Channel "A" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "A" data channel. In all three speeds, this signal generates the secondary side signal, normally connected to RJ-45 pin 2. In 100BASE-FX mode, it is connected instead to the negative SFP transmit data signal (SFP_TD–). See Section 9: "System Schematics" for details.
A8	TXVPB	A_{DIFF}	**TX/RX Channel "B" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "B" data channel. In all three speeds, this signal generates the secondary side signal, normally connected to RJ-45 pin 3. In 100BASE-FX mode, it is connected instead to the positive SFP receive data signal (SFP_RD+). See Section 9: "System Schematics" for details.
B8	TXVNB	A_{DIFF}	**TX/RX Channel "B" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "B" data channel. In all three speeds, this signal generates the secondary side signal, normally connected to RJ-45 pin 6. In 100BASE-FX mode, it is connected instead to the negative SFP receive data signal (SFP_RD–). See Section 9: "System Schematics" for details.
A7	TXVPC	A_{DIFF}	**TX/RX Channel "C" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "C" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 4 (not used in 10M/100M modes). See Section 9: "System Schematics" for details.
B7	TXVNC	A_{DIFF}	**TX/RX Channel "C" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "C" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 5 (not used in the 10M/100M modes). See Section 9: "System Schematics" for details.
A6	TXVPD	A_{DIFF}	**TX/RX Channel "D" Positive Signal.** Positive differential signal connected to the positive primary side of the transformer. This signal forms the positive signal of the "D" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 7 (not used in the 10M/100M modes). See Section 9: "System Schematics" for details.
B6	TXVND	A_{DIFF}	**TX/RX Channel "D" Negative Signal.** Negative differential signal connected to the negative primary side of the transformer. This signal forms the negative signal of the "D" data channel. In 1000Mb mode, this signal generates the secondary side signal, normally connected to RJ-45 pin 8 (not used in the 10M/100M modes). See Section 9: "System Schematics" for details.

Table 13. Power Supply and Ground Connections

100 TFBGA BALL	Supply Name	Recommended PCB Power Plane	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Supply Pins					
H4	VDDIO[1]	V+IO	P	3.3V or 2.5V	Power for the RXLOS/SIGDET and MODDEF0/CLKOUT pins
H8	VDDIOMICRO[1]	V+IO	P	3.3V or 2.5V	Power for SMI and EEPROM Interface
C4	VDDIOCTRL[1]	V+IO	P	3.3V or 2.5V	Power for JTAG I/O
Digital Core Power Supply Pins					
G10,F3,G3, F8,H7	VDD12	V+12	P	1.2V	Power for internal digital logic, PLL and SerDes/SGMII I/O Power
Analog Power Pins					
C8,D9	VDD33A	V+33A	P	3.3V	Power for MDI, CMODE, PLL, and LED blocks
C9	VDDREG	V+33REG	P	3.3V	Power for on-chip switching regulator
E9	VDD12A	V+12A	P	1.2V	Power for internal PLL and ADC
Ground Pins					
D4,D5,D6, D7,E4,E5, E6,E7,F4, F5,F6,F7, G4,G5,G6, G7,C6,C7, D8,E8,H6	VSS	GND	G	0V	Ground for all blocks

[1] The I/O power supplies on the PHY are separated on the chip itself to facilitate support for different VDDIO supply voltages. These VDDIO supplies can be run independently at 2.5V OR 3.3V I/O.

Table 14. No Connects

100 TFBGA BALL	Signal Name	Type	Description
C1,D1,E1, F1,G1,H1, J1,K1,D2, E2,F2,G2, H2,J2,K2, H3,J3,K3, J4,K4,H5, J5,K5,J6,K6	NC	NC	**No Connect - must be left floating**

Table 15. Power Supply and Associated Functional Signals

Power Supply Pins	Nominal Voltages	Associated Functional Pins
VDDIO	3.3V or 2.5V	RXLOS/SIGDET, MODDEF0/CLKOUT
VDDIO-MICRO	3.3V or 2.5V	EECLK/PLLMODE, EEDAT, TXDIS/$\overline{\text{SRESET}}$, $\overline{\text{MDINT}}$, MODDEF1/MDC, MODDEF2/MDIO, CLKOUTMICRO/$\overline{\text{OSCDIS}}$
VDDIO-CTRL	3.3V or 2.5V	$\overline{\text{RESET}}$, TDO, TDI, TMS, TCK, $\overline{\text{TRST}}$
VDD33A	3.3V	LED[2:0], CMODE[3:0], TXVND, TXVPD, TXVNC, TXVPC, TXVNB, TXVPB, TXVNA, TXVPA, XTAL2, XTAL1/REFCLK, REFFILT, REFREXT
VDDREG	3.3v	REGOUT
VDD12	1.2V	RDP, RDN, TDP, TDN, SCLKP, SCLKN
VDD12A	1.2V	

9 SYSTEM SCHEMATICS

9.1 System Schematic – SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode

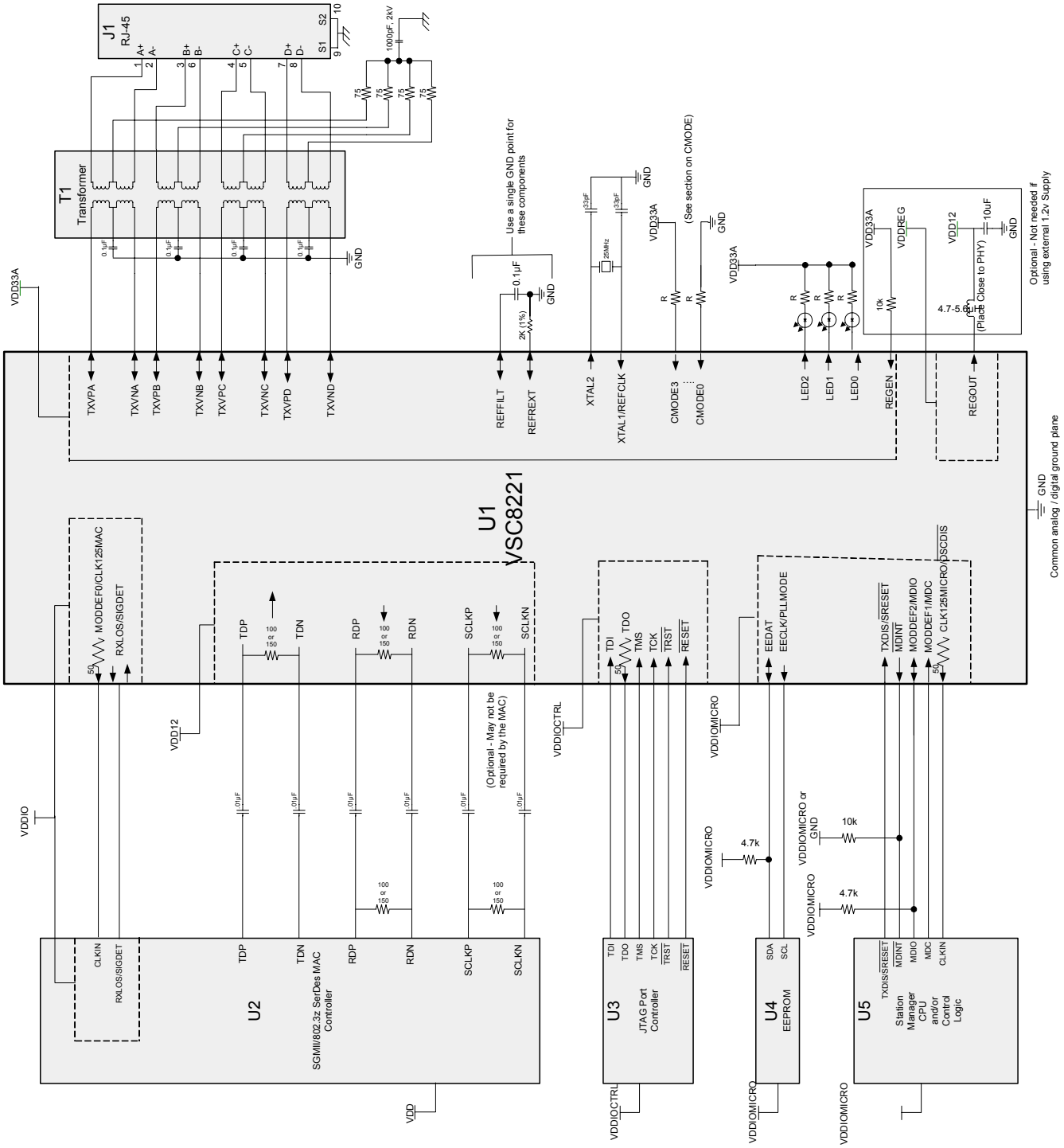


Figure 4. System Schematic – SGMII/802.3z SerDes MAC to 1000Mbps CAT5 Media PHY Operating Mode

9.2 System Schematic – 100Mbps Fiber Media Implementation

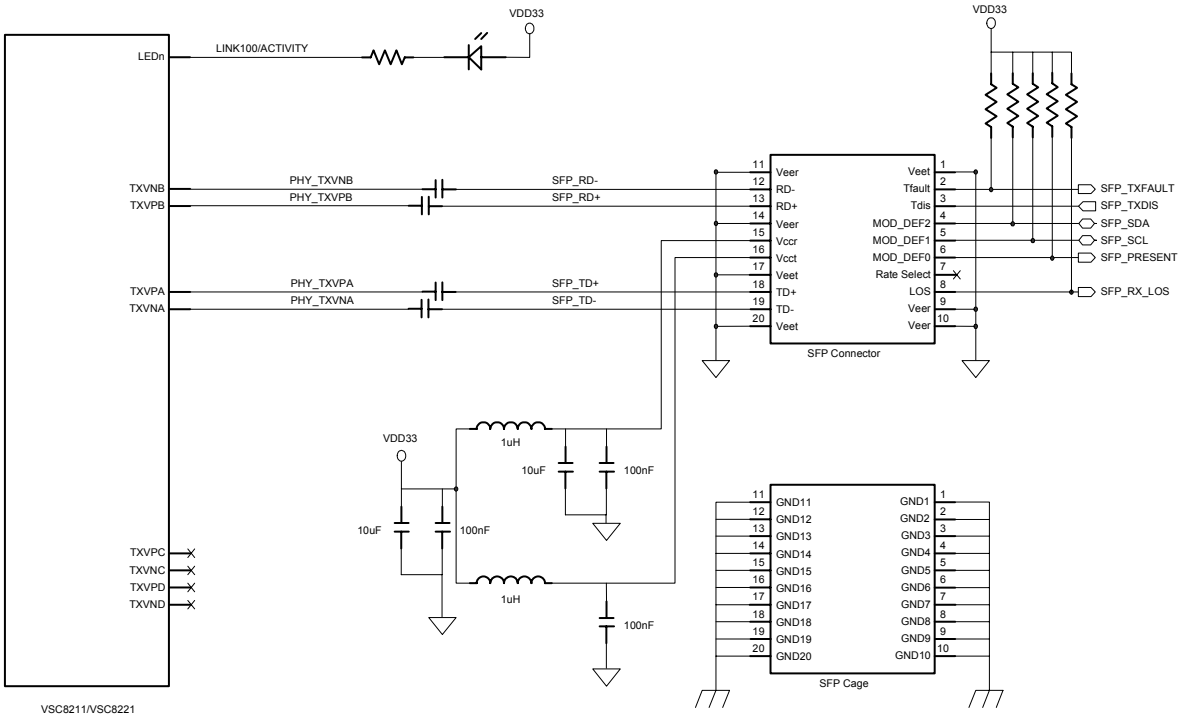


Figure 5. System Schematic – 100Mbps Fiber Media Implementation

10 TWISTED PAIR INTERFACE

The twisted pair interface on the VSC8221 is fully compliant with the IEEE802.3-2000 specification for CAT-5 media. All passive components necessary to connect the PHY to an external 1:1 transformer have been integrated into the VSC8221. The connection of the twisted pair interface is shown in the following figure:

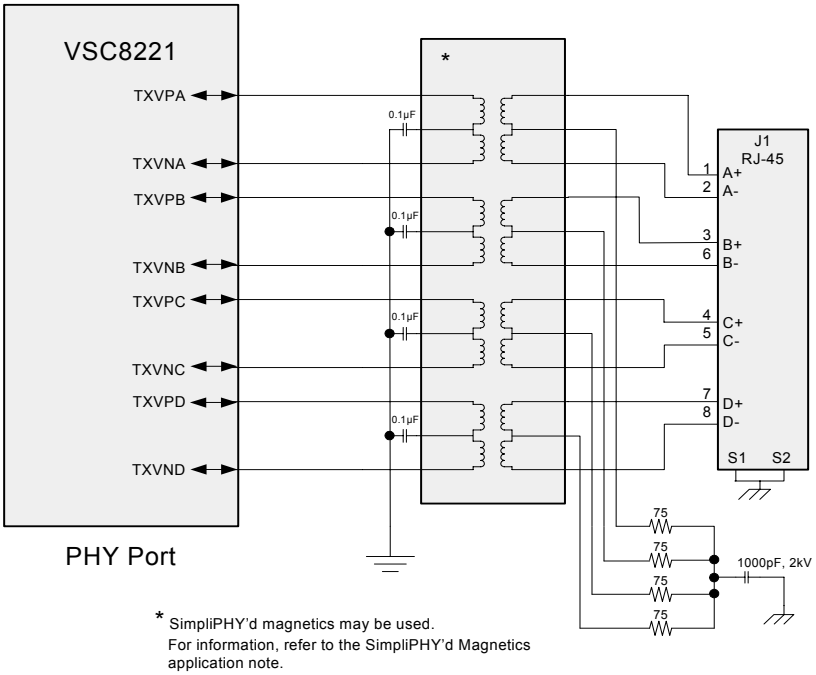


Figure 6. Twisted Pair Interface

Unlike other Gigabit PHYs, which do not integrate the line terminations in the PHY, the VSC8221's twisted pair interface is compatible with a wide variety of standard magnetics and RJ-45 modules from common module vendors. Depending upon the application (the number of ports, EMI performance requirements such as FCC Class A or B, the type and quality of the equipment shielding, and other EMI design practices, for example), the twisted pair interface may be used with standard (12- or 8-core) magnetics as well as SimpliPHY'd (4-core) magnetics modules available from many module vendors. In addition, this interface is also used to provide support for 100Mbps fiber module connection. For more information on the suitability of using SimpliPHY'd magentics for a particular design, see the *Magnetics Guide*, available from the Vitesse Web site.

10.1 Twisted Pair Auto-Negotiation (IEEE802.3 Clause 28)

The VSC8221 supports twisted pair auto-negotiation, as defined in IEEE 802.3-2002 clause 28. (However, auto-negotiation is not defined by IEEE for the 100BASE-FX mode and is therefore not supported.) This process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Auto-negotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard. If the link partner does not support auto-negotiation, the VSC8221 will automatically use parallel-detect to select the appropriate link speed.

Clause 28 twisted-pair auto-negotiation can be disabled by clearing MII Register 0.12 – Auto-Negotiation Enable. If auto-negotiation is disabled, the operating speed and duplex mode of the VSC8221 is determined by the state of MII Register 0.13, 0.6 – Forced Speed Selection and MII Register 0.8 – Duplex Mode.

10.2 Twisted Pair Auto MDI/MDI-X Function

For trouble-free configuration and management of Ethernet links, the VSC8221 includes robust Automatic Crossover Detection functionality for all three speeds on the twisted pair interface (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with

the IEEE standard. In addition, the VSC8221 detects and corrects polarity errors on all MDI pairs, beyond what is required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default. However, complete user control of these two features is contained in MII Register bits 18.5:4. Status bits for each of these functions are indicated in MII Register 28 (1Ch) – Auxiliary Control and Status Register.

The VSC8221's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table:

Table 16. MDI Wiring Pair Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by VSC8221	A	B	C	D	Normal MDI mode Normal DTE/NIC mode No crossovers
	B	A	C	D	MDI-X mode Normal for switches & repeaters Crossover on A and B pairs only
	A	B	D	C	Normal MDI mode Normal for DTEs (NICs) No crossovers Pair swap on C and D pairs
	B	A	D	C	Normal MDI-X mode Normal switch/repeater mode Crossovers assumed Crossover on A and B pairs Pair swap on C and D pairs

10.3 Auto MDI/MDI-X in Forced 10/100 Link Speeds

The VSC8221 includes the ability to perform Auto MDI/MDI-X even when auto-negotiation is disabled (MII Register 0.12 = 0) and the link is forced into 10/100 link speeds. In order to enable this feature, additional MII register write settings are also needed in the following order:

To enable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x52b5
- Write MII Register 18 = 0x0012
- Write MII Register 17 = 0x2803
- Write MII Register 16 = 0x87fa
- Write MII Register 31 = 0x0000

To disable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x52b5
- Write MII Register 18 = 0x0012
- Write MII Register 17 = 0x3003
- Write MII Register 16 = 0x87fa
- Write MII Register 31 = 0x0000

10.4 Forcing the PHY into MDI or MDI-X mode in 10/100/1000 Link Speeds

If the Auto-MDI/MDI-X feature is disabled by setting MII Register 18.5, or by disabling auto-negotiation, the PHY's default behavior is to establish a link in MDI mode. To force the PHY into MDI-X mode:

- Write MII Register 31 = 0x2A30
- Write MII Register 5 = 0x1038
- Write MII Register 31 = 0x0000

To force the PHY into MDI mode:

- Write MII Register 31 = 0x2A30
- Write MII Register 5 = 0x1030
- Write MII Register 31 = 0x0000

To disable the forcing of MDI/MDI-X mode:

- Write MII Register 31 = 0x2A30
- Write MII Register 5 = 0x1020
- Write MII Register 31 = 0x0000

10.5 Twisted Pair Link Speed Downshift

In addition to automatic crossover detection, the VSC8221 supports an automatic link speed "downshift" option for operation in cabling environments incompatible with 1000BASE-T. When this feature is enabled, the VSC8221 will automatically change its auto-negotiation advertisement to 100BASE-TX after a set number of failed attempts at 1000BASE-T. This is especially useful in setting up networks using older cable installations which may include only pairs A and B and not pairs C and D. The link speed downshift feature is configured and monitored through MII Register 20E (14h) - Extended PHY Control Register #3.

10.6 100Mbps Fiber Support Over Copper Media Interface

The VSC8221 supports 100BASE-FX over its copper media interface by using pairs A and B, which provide TX and RX differential connections, respectively. If the fiber module does not have internal AC coupling capacitors, then they are required between the PHY and fiber module. The value should be 0.1µF.

The RXLOS/SIGDET signal is not used in this mode.

A separate 1000BASE-X fiber module may be connected to the PHY through the 1000BASE-X SerDes pins.

10.6.1 Register Settings

The PHY can be brought into the 100BASE-FX operation mode using the following configuring sequence:

1. Initialize the PHY into the specific MAC-to-copper operating mode for the MAC interface type required (register 23).
2. Disable auto-negotiation and force the 100BASE-T FDX mode (register 0).
3. Run the 100BASE-FX initialization script; for more information, see Section 31.10: "100BASE-FX Initialization Script".
4. Configure other settings, such as LEDs.

11 TRANSFORMERLESS OPERATION FOR PICMG 2.16 AND 3.0 IP-BASED BACKPLANES

The twisted pair interface supports capacitively coupled links, such as those specified by the PICMG 2.16 and 3.0 specifications. With proper AC coupling, the typical category-5 magnetic isolation can be replaced with capacitors. Refer to Vitesse Application Note #3 (AN003 - Transformerless Ethernet Concept and Applications) for more information. See MII Register Bit 24.12 for more information.

By enabling the PICMG Miser mode, power consumption can be reduced to under 500mW.

12 DUAL MODE SERIAL MANAGEMENT INTERFACE (SMI)

The Serial Management Interface provides access to the PHY registers for device configuration and Status Information. It also provides access to the EEPROM connected to the EEDAT and EECLK pins (EEPROM Interface) of the PHY. For details on EEPROM access through the SMI interface, refer to Section 19 on page 57.

The MODDEF1/MDC, MODDEF2/MDIO, and $\overline{\text{MDINT}}$ pins comprise the SMI interface.

By writing to MII Register 21E.15 at startup (Refer to Section 18 on page 53 and Section 19 on page 57 for details), the SMI of the PHY can be set to operate in one of the following two modes:

1. MSA
2. IEEE

12.1 PHY Register Access with SMI in MSA mode

In this mode, the PHY registers are accessed using the standard MSA compliant protocol. This protocol is generally used for reading and writing to Atmel's AT24 series compatible EEPROMs.

In this mode, the SMI pins function as follows:

Table 17. SMI Pin Descriptions - MSA Mode

Pin Name	Description
MODDEF1	Clock Input. Connect to the SCL pin of the AT24 series of EEPROMs.
MODDEF2	Bidirectional Data. Connect to the SDA pin of the AT24 series of EEPROMs. This pin should be pulled high on the board using a 4.7kΩ to 10kΩ pullup resistor.
$\overline{\text{MDINT}}$	Interrupt Signal.

According to the protocol described in the MSA specification, the following conditions are defined:

- **Start [S]:** A high to low transition on the MODDEF2 pin when MODDEF1 is high.
- **Data [D]:** A transition on the MODDEF2 pin when MODDEF1 is low. A low to high transition is '1' and a high to low transition is '0'.
- **Stop [T]:** A low to high transition on the MODDEF2 pin when MODDEF1 is high.
- **Acknowledge (By Receiver) [A]:** A low driven by the PHY/Receiver after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The host does not drive the MODDEF2 Data line in this condition.
- **Acknowledge (By Host) [H]:** A low driven by the host after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The PHY/Receiver does not drive the MODDEF2 Data line in this condition.
- **No Acknowledge (By Host) [N]:** A high driven by the host after 8 Data states. The transition on MODDEF2 takes place when MODDEF1 is low. The PHY/Receiver does not drive the MODDEF2 Data line in this condition

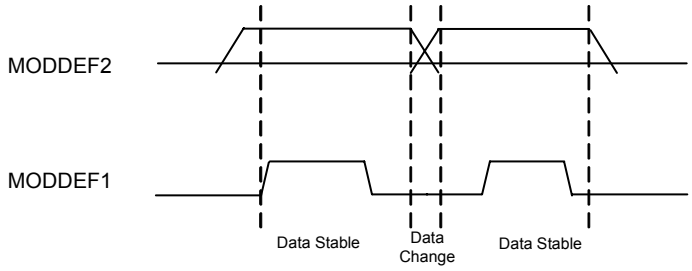


Figure 7. Data Validity [D]

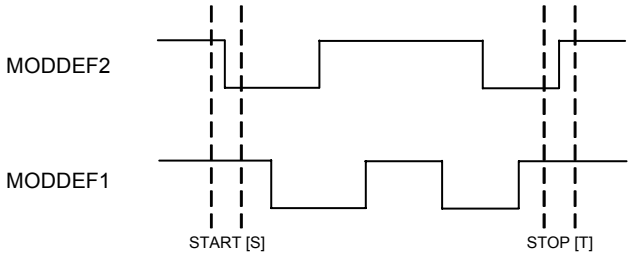


Figure 8. Start [S] and Stop [T] Definition

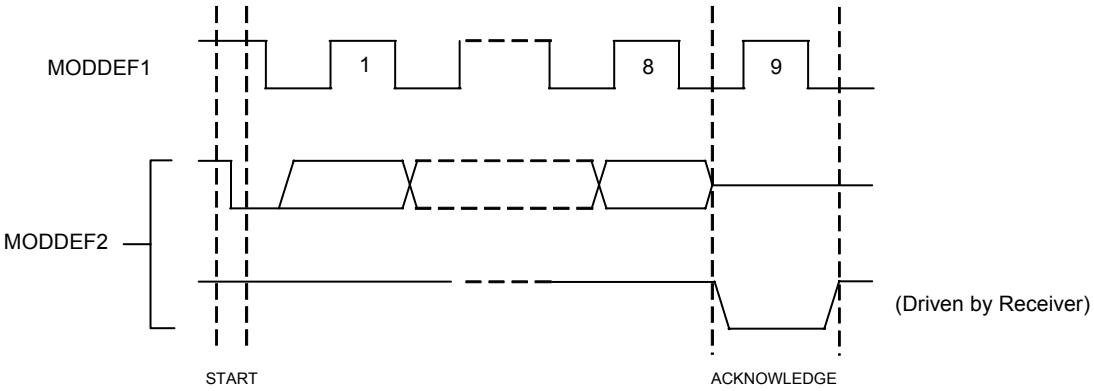


Figure 9. Acknowledge (by Receiver) [A]

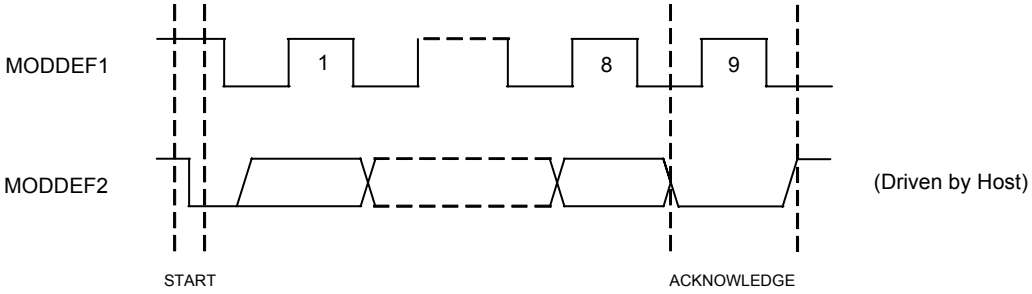


Figure 10. Acknowledge (by Host) [H]

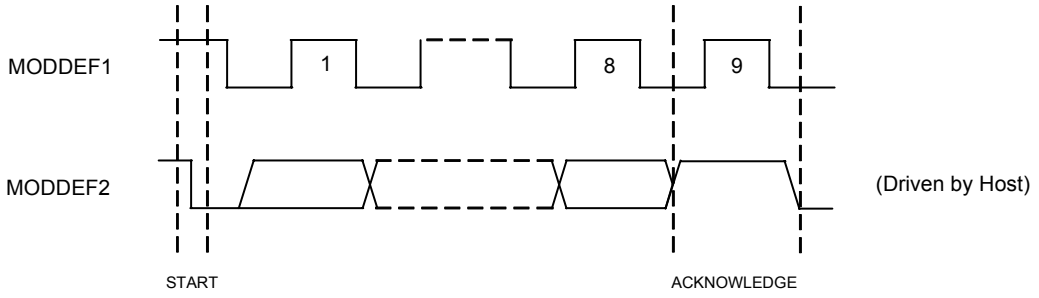
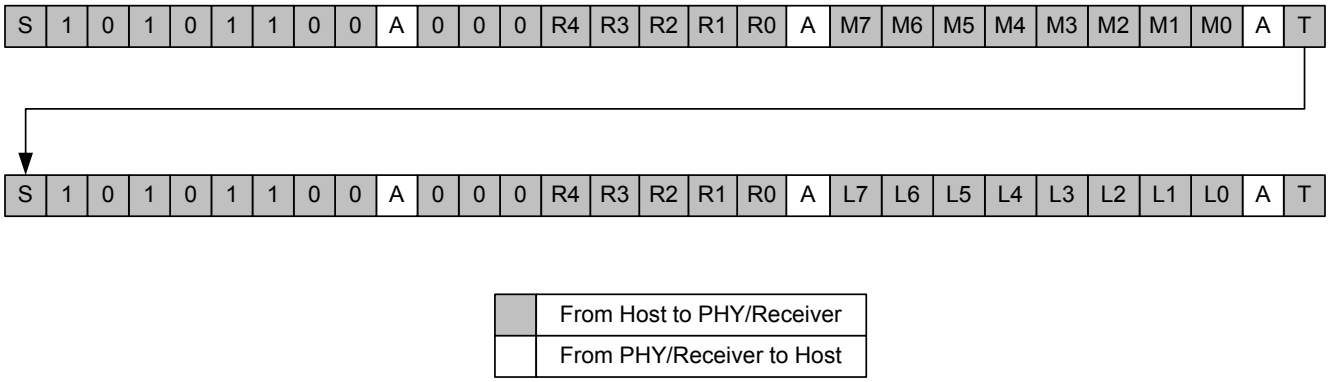


Figure 11. No Acknowledge (by Host) [N]

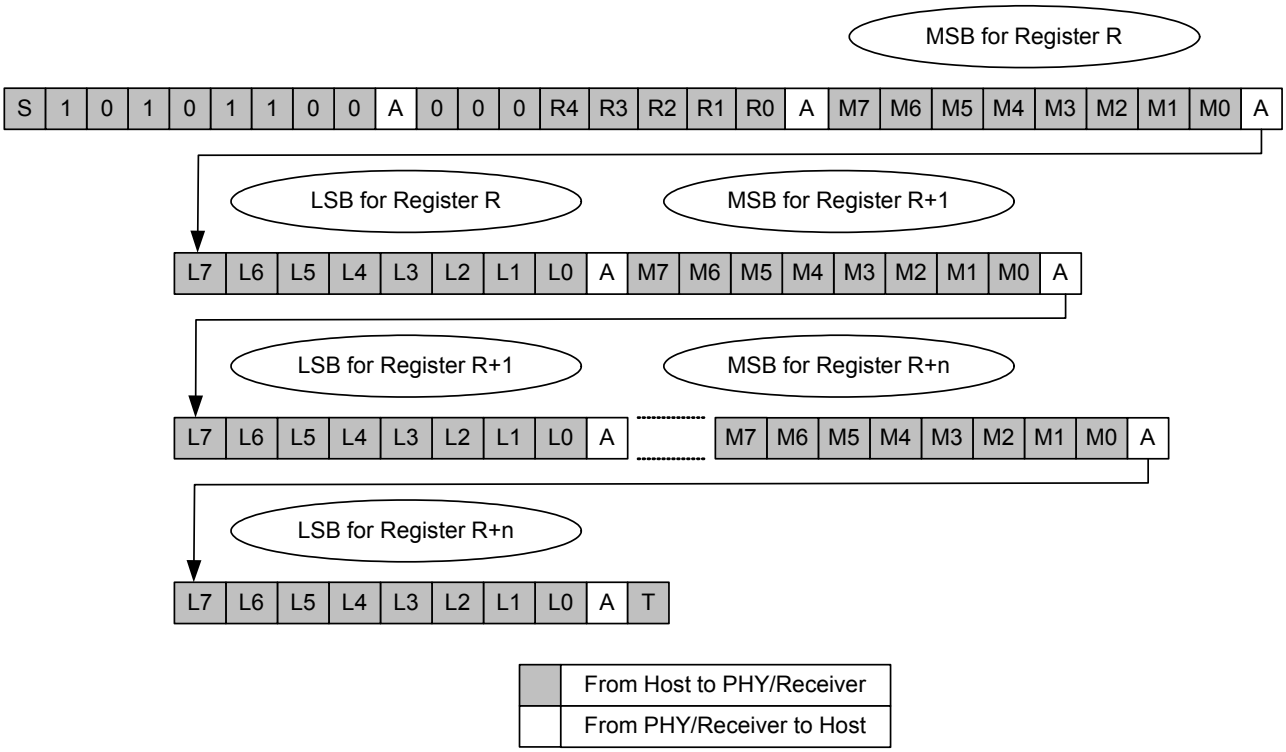
12.1.1 Write Operation - Random Write



- R4..R0 are the 5 bits of the Register address R.
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Upper byte of the 16 bit Register data

The PHY register is written only after the host performs the lower data byte write operation.

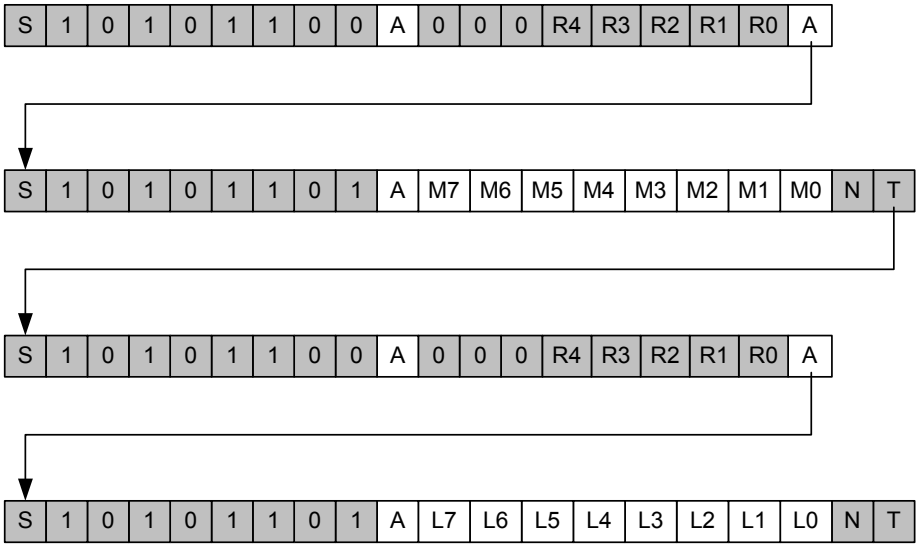
12.1.2 Write Operation - Sequential Write



- R4..R0 are the 5 bits of the Register address R.
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Upper byte of the 16 bit Register data

The PHY register is written only after the host performs the lower data byte write operation.

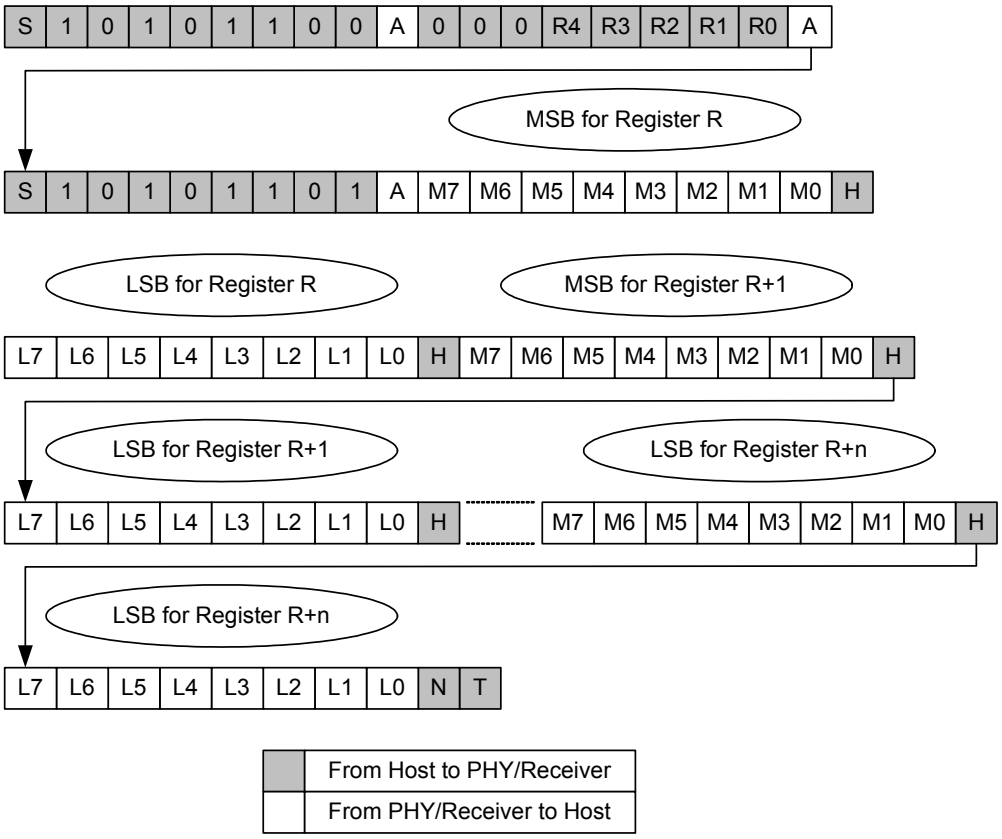
12.1.3 Read Operation - Random Read



	From Host to PHY/Receiver
	From PHY/Receiver to Host

- R4..R0 are the 5 bits of the Register address
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Lower byte of the 16 bit Register data

12.1.4 Read Operation - Sequential Read



- R4..R0 are the 5 bits of the Register address
- M7..M0 are bits of the Upper byte of the 16 bit Register data
- L7..L0 are bits of the Lower byte of the 16 bit Register data

12.2 PHY Register Access with SMI in IEEE Mode

In IEEE mode, the SMI is fully compliant with the IEEE 802.3-2000 MII Interface specifications.

In IEEE mode, the SMI pins function as follows:

Table 18. SMI Pin Descriptions - IEEE Mode

Pin Name	Description
MDC	Clock Input, 0 – 12.5 Mhz.
MDIO	Bidirectional Data. This pin should be pulled high on the board using a 4.7kΩ to 10kΩ resistor.
$\overline{\text{MDINT}}$	Active Low or Active High open drain interrupt output.

As many as 32 PHYs (32 distinct PHY Addresses) can share a common IEEE SMI signal pair (MDC, MDIO).

Data is transferred over the IEEE SMI using 32-bit frames with an optional and arbitrary length preamble. The IEEE SMI frame format is described in the following table.

Table 19. SMI Frame Format

	Direction from VSC8221	Preamble	Start of Frame	Op Code	PHY Address	Register Address	Turn-Around	Data	Idle
# of bits		1+	2	2	5	5	2	16	?
Read	Output	Z's	ZZ	ZZ	Z's	Z's	Z0	data	Z's
	Input	1's	01	10	addr	addr	ZZ	Z's	Z's
Write	Output	Z's	ZZ	ZZ	Z's	Z's	ZZ	Z's	Z's
	Input	1's	01	01	addr	addr	10	data	Z's

- Idle: During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical "1" state. Since idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.
- Preamble: For the VSC8221, the preamble is optional. By default, preambles are not expected or required. The preamble is a string of "1"s. If it exists, the preamble must be at least one bit, but otherwise may be arbitrarily long. See MII Register 1.6 for more information.
- Start of Frame: A "01" pattern indicates the start of frame. If these bits are anything other than "01", all following bits are ignored until the next "preamble:0" pattern is detected.
- Operation Code: A "10" pattern indicates a read. A "01" pattern indicates a write. If these bits are anything other than "01" or "10", all following bits are ignored until the next "preamble:0" pattern is detected.
- PHY Address: The next five bits are the PHY address. The PHY responds to a message frame only when the received PHY address matches its physical address. The PHY's address is indicated by the CMODE1[2] and CMODE0[3:0] bits.
- Register Address: The next five bits are the register address.
- Turn-Around: The next two bits are "turn-around" (TA) bits. They are used to avoid contention when a read operation is performed on the MDIO. During read operations, the VSC8221 will drive the second TA bit, which is a logical "0".
- Data: The next sixteen bits are data bits. When data is being read from the PHY, data is valid at the output of the PHY from one rising edge of MDC to the next rising edge of MDC. When data is being written to the PHY, data must be valid around the rising edge of MDC.
- Idle: The sequence is repeated.

The following two figures diagram IEEE SMI read and IEEE SMI write operations.

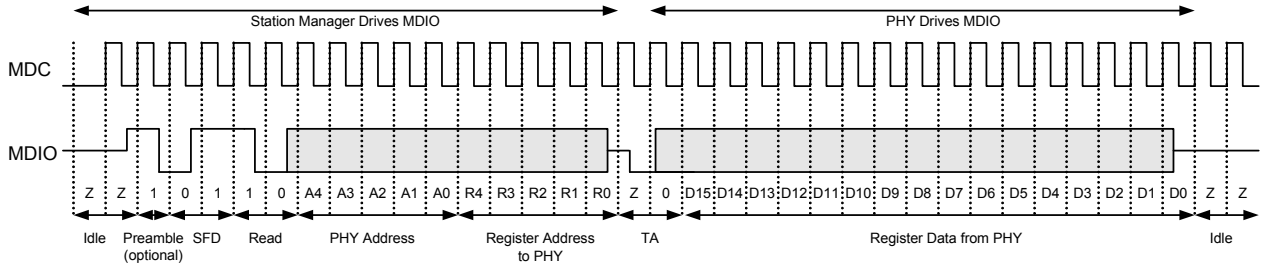


Figure 12. MDIO Read Frame

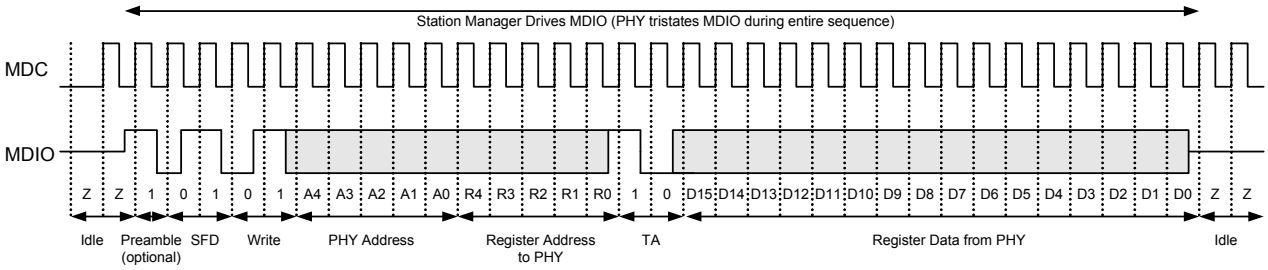


Figure 13. MDIO Write Frame

12.3 SMI Interrupt

The SMI includes an output signal $\overline{\text{MDINT}}$ for signaling the Station Manager when certain events occur in the PHY. The $\overline{\text{MDINT}}$ pin can be configured for active-low or active-high operation by tying the pin to either a pull-up resistor to VDDIOMICRO or to a pull-down resistor to GND.

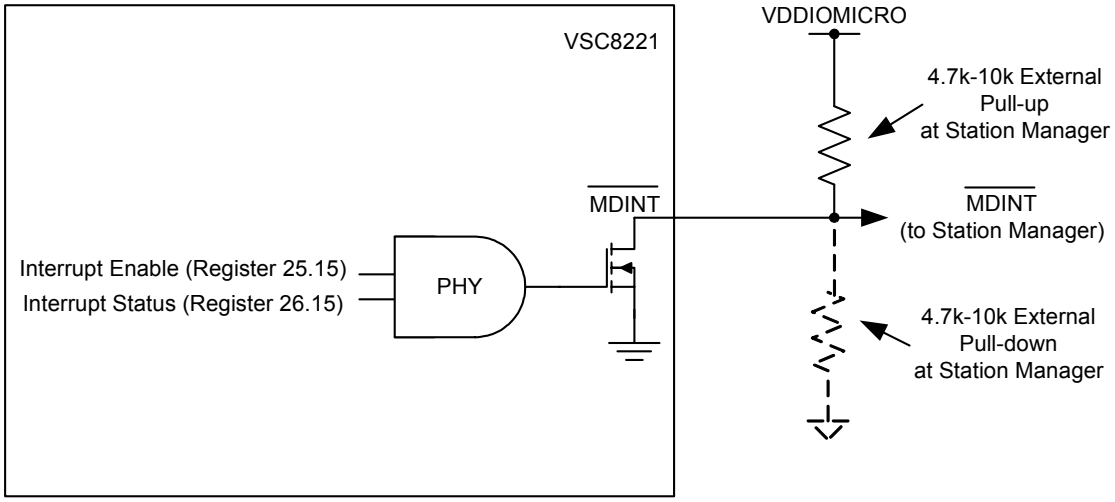


Figure 14. Logical Representation of $\overline{\text{MDINT}}$ Pin

13 LED INTERFACE

The PHY has dedicated pins LED[2:0] to drive 3 LEDs directly. For power savings, all LED outputs can be configured to pulse at 5kHz with a 20% duty cycle. All LED outputs are active-low and driven with 3.3V from the VDD33A power supply when deasserted.

Because the 100BASE-FX mode uses 100BASE-T resources, its indications are those of the 100BASE-T mode.

Four different functions have been assigned to each LED pin. Selection is done through CMODE hardware configuration (see Section 18 on page 53) or through MII Register 27 (1Bh) – LED Control Register. The functions are assigned according to the following table:

Table 20. LED Function Assignments

LED Configuration Bits	Value	LED Function Selection
LED Pin 2 Config [1:0]	11	TX[1]
	10	Link/Activity
	01	Duplex/Collision[2]
	00	Link10/Activity
LED Pin 1 Config [1:0]	11	Link100/1000/Activity[1]
	10	Link/Activity
	01	Link10/100/Activity[2]
	00	Link100/Activity
LED Pin 0 Config [1:0]	11	RX[1]
	10	Fault
	01	Link/Act (with serial output on LED pins 1 and 2)[2]
	00	Link1000/Activity

[1] When using Enable Force LED in MII Register 20E.13, this setting is “Force on”. For more information, see Section 23.3.5 on page 100.
[2] When using Enable Force LED in MII Register 20E.13, this setting is “Force Off”. For more information, see Section 23.3.5 on page 100.

LED functions are summarized in the following table:

Table 21. Parallel LED Functions

Function Name	State	Description
Link1000/Activity[1]	1	No link in 1000BASE-T or 1000BASE-X
	0	Valid 1000BASE-T link or 1000BASE-X link
	Pulse-stretch/Blink[2]	Valid 1000BASE-T link and activity present (optional)
Link100/Activity[1]	1	No link in 100BASE-Tx
	0	Valid 100BASE-Tx link
	Pulse-stretch/Blink[2]	(optional) Valid 100BASE-Tx link and activity present

Table 21. Parallel LED Functions *(continued)*

Function Name	State	Description
Link10/Activity[1]	1	No link in 10BASE-T
	0	Valid 10BASE-T link
	Pulse-stretch/Blink[2]	(optional) Valid 10BASE-T link and activity present
Link10/100/ Activity[1]	1	No link in 10BASE-T or 100BASE-Tx
	0	Valid 10BASE-T link or valid 100BASE-Tx link
	Pulse-stretch/Blink[2]	(optional) Valid 10BASE-T link or valid 100BASE-Tx link and activity present
Link100/1000/ Activity[1]	1	No link in 100BASE-Tx or 1000BASE-T
	0	Valid 100BASE-Tx link or valid 1000BASE-T link
	Pulse-stretch/Blink[2]	(optional) Valid 100BASE-Tx link or valid 1000BASE-T link and activity present
Link/Act[3]	1	No link in any speed
	0	Valid link in any speed
	Pulse-stretch/Blink[2]	Valid link in any speed and activity present
Collision	1	No collisions detected
	Pulse-stretch/blink[2]	Collisions detected
Activity	1	No activity
	Pulse-stretch/blink[2]	Activity present
Fiber	1	No valid 1000BASE-X link established
	0	Fiber media detected on SerDes interface and valid 1000BASE-X link established
Fault	1	No IEEE Clause 37/28 auto-negotiation fault
	0	IEEE Clause 37/28 auto-negotiation fault
Serial	**	See serial interface specification
Duplex/Collision[4]	1	Link established in half-duplex mode, or no link established
	0	Link established in full-duplex mode
	Pulse-stretch/Blink[2]	(optional) Link established in half duplex mode and collisions present
Rx	1	No activity on Rx side
	Pulse-stretch/blink[2]	Activity present on Rx side
Tx	1	No activity on Tx side
	Pulse-stretch/blink[2]	Activity present on Tx side

[1] The “Linkxxx” functions are combined with “Activity” by default. To use the LED as a dedicated “Linkxxx,” LED MII register bit 27.1 must be set.
[2] Function can either blink or be pulse-stretched when active. See Table 22 below.
[3] The “Link” functions are combined with “Activity” by default. To use the LED as a dedicated “Link,” LED MII Register bit 27.2 must be set.
[4] The “Duplex” function is combined with “Collision” by default. To use the LED as a dedicated “Duplex,” LED MII register bit 27.0 must be set.

In addition to function selection, several options are available for the LED outputs through the use of MII register 27.5:0. These are summarized below:

Table 22. LED Output Options

MII Reg Bits	LED Option Bits	LED Function Selection
5	LED Pulse-stretch Rate/ Blink Rate	0 = 5 Hz blink rate/200 ms pulse-stretch 1 = 10 Hz blink rate/100 ms pulse-stretch
4	LED Pulsing Enable	1 = Enable 5 kHz, 20% duty cycle LED pulsing for power savings 0 = LED pulsing disabled
3	LED Pulse-Stretch / Blink Select	1 = Collision, Activity, Rx and Tx functions will flash at a rate selected by Blink/Pulse-Stretch Rate bits 0 = Collision, Activity, Rx and Tx functions will blink at a rate selected by Blink/Pulse-Stretch Rate bits
2	Link/Activity Behaviour	1 = Link function indicates link status only 0 = Link/Activity function will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.
1	LED Linkxxxx/Activity[1] Behavior	1 = Link function indicates link status only 0 = All link functions will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.
0	LED Duplex/Collision Behavior	1 = Duplex function indicates duplex status only 0 = Duplex function will blink or flash when collision is present

[1] Linkxxxx/Activity stands for Link10/Activity,Link100/Activity,Link1000/Activity,Link10/100/Activity and Link100/1000/Activity. Its definition does not include the Link/Activity function.

13.1 Serial LED Output

A serial output option is available which allows access to all LED signals through two pins. This option is selected by setting LED Pin 0 configuration bits to 01 on the PHY. In this mode, LED pins 1 and 2 function as serial data and clock. LED function outputs for the PHY are clocked out on the rising edge of data clock. The clock rate is approximately 1MHz.

The serial bitstream outputs each LED signal as described by the numbered list below.The individual signals shall be clocked out in the following order:

1. Link1000/Act
2. Link/Act
3. Link100/Act
4. Act
5. Link10/Act
6. Dup/Col
7. Tx
8. Col
9. Rx
10. Fault
11. Fiber/Copper

14 TEST MODE INTERFACE (JTAG)

The PHY supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 compliant test interface, often referred to as a “JTAG TAP Interface”. IEEE 1149.1 defined test logic provides the following standardized test methodologies:

- Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate.
- Testing the integrated circuit itself during IC and systems manufacture.
- Observing or modifying circuit activity during the component’s normal operation.

The JTAG Test interface logic on the PHY, accessed through a Test Access Port (TAP) interface, consists of a boundary- scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal $\overline{\text{TRST}}$.

The following figure diagrams the TAP and Boundary Scan Architecture.

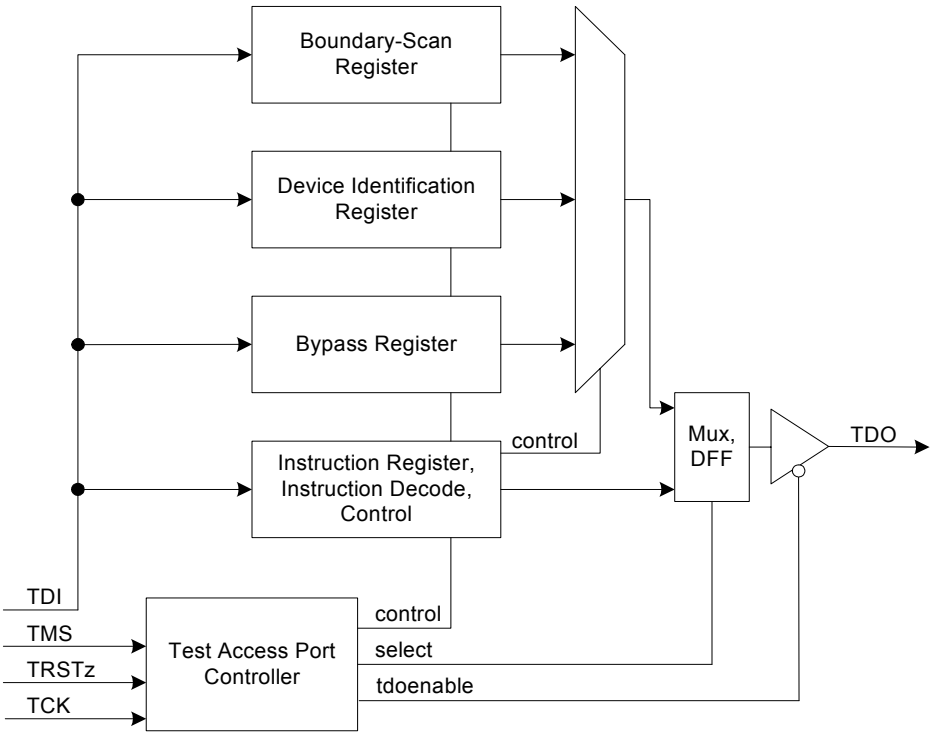


Figure 15. Test Access Port and Boundary Scan Architecture

The PHY also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number, and version number of the device to be determined through the TAP Controller. See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 23. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Vitesse’s Manufacturer Identity	LSB
Bit Field	31 - 28	27 - 12	11 - 1	0
Binary Value	0001	1000 0010 0010 0001	001 1001 1000	1

14.1 Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The VSC8221 supports the instruction codes listed in the following table and described below.

Table 24. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	0000	Boundary-Scan Register	72	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	0001	Boundary-Scan Register	72	Mandatory IEEE 1149.1
IDCODE	0110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	0010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	0011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	0111	Bypass Register	1	Mandatory IEEE 1149.1
Reserved	0100, 1000, 1001, 1010, 1011, 1100, 1101,1110, 1111			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.[1]

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), part number (bits 27:12), and Vitesse's manufacturer identity (bits 11:1) to be serially read from the PHY.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[1]

HIGHZ
The optional HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.[1]

[1]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

BYPASS

The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

14.2 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control. The full boundary scan cell order is available from Vitesse Semiconductor in *.BSD file format.

15 ENHANCED ACTIPHY POWER MANAGEMENT

In addition to the IEEE-specified power-down control bit (MII Register 0.11), the VSC8221 implements an Enhanced ActiPHY™ power management mode. This mode enables support for power-sensitive applications by utilizing a signal-detect function that monitors the media interface for the absence of a link to determine when to automatically power-down the PHY. The Station Manager is in control of this mode. The PHY then 'wakes up' at a programmable interval and attempts to 'wake-up' the link partner PHY by sending a fast link pulse (FLP) on the Media Interface.

The Enhanced ActiPHY™ power management mode can be set at startup (Refer to Section 18 on page 53 and Section 19 on page 57 for details) or at any time during normal operation by writing to MII Register 28.6.

15.1 Operation in Enhanced ActiPHY Mode

There are three PHY operating states when Enhanced ActiPHY™ mode is enabled:

- Low power state
- LP Wake up state
- Normal operating state (link up state)

The PHY switches between the low power state and LP wake up state at a programmable rate (sleep timer) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. When the PHY is in the normal operating state and link is lost, the PHY returns to the low power state after the link status timeout timer has expired. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY™ state machine will operate as described above. If auto-negotiation is disabled and the link is forced to 10BT or 100BTX mode while the PHY is in the low power state, the PHY continues to transition between the low power and LP wakeup states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

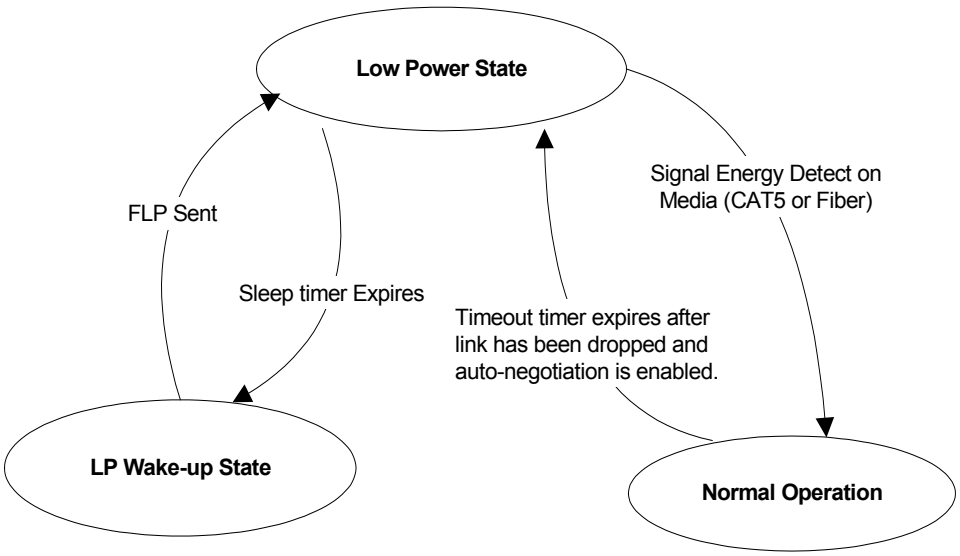


Figure 16. Enhanced ActiPHY State Diagram

15.2 Low-Power State

In the low-power state, all major digital blocks are powered down. However the following functionality is provided:

- SMI interface (MDC/MODDEF1, MDIO/MODDEF2, $\overline{\text{MDINT}}$)
- CLKOUT and CLKOUTMICRO

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of the low power state and transitions to the Normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Auto-negotiation incapable (blind/forced) 100BTX only link partner
- Auto-negotiation incapable (blind/forced) 10BT only link partner
- Another PHY in enhanced ActiPHY LP wakeup state

In the absence of signal energy on the media pins, the PHY will transition from the low power state to the LP Wake up state periodically based on the programmable sleep timer. Two register bits (MII Register bits 28.1:0) are provided to program the value of the sleep timer. The sleep timer can be programmed to 2'b00 (1sec), 2'b01 (2sec), 2'b10 (3sec), or 2'b11 (4sec). The default value is 2 seconds. The actual sleep time duration is randomized by -80ms to +60ms to prevent two PHYs in Enhanced ActiPHY mode from entering a lock-up state.

15.3 LP Wake-Up State

In this state, the PHY attempts to wake up the link partner. One complete FLP (Fast link Pulse) is sent on both pairs A and B of the CAT5 media. In this state, the following functionality is provided:

- SMI interface (MDC/MODDEF1, MDIO/MODDEF2, $\overline{\text{MDINT}}$)
- CLKOUT and CLKOUTMICRO

After sending signal energy on the relevant media, the PHY returns to the Low power state.

15.4 Normal Operating State

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration programmed through a link status timeout timer and then enters the low power state. The Link Status Timeout timer can be programmed to 2'b00 (1sec), 2'b01 (2sec), 2'b10 (3sec) or 2'b11 (4sec). The default value for this timer is 2 seconds.

16 Ethernet In-line Powered Device Support

16.1 Cisco In-Line Powered Device Detection Mode

Used to detect in-line powered devices and devices that derive power from CAT-5 cable for their operation in Ethernet network applications, the VSC8221 device's in-line powered device detection mode can be part of a system that allows IP-phones and other devices to receive power from an Ethernet cable, similar to office digital phones receiving power from a PBX (Private Branch Exchange) office switch via the phone cable. This can eliminate the need for an IP-Phone to have an external power supply, since the Ethernet cable provides power. It also enables the in-line powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, etc.). This mode is disabled by default and must be enabled in order to perform in-line powered device detection. Please refer to http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml for additional information.

16.2 In-Line Power Ethernet Switch Diagram

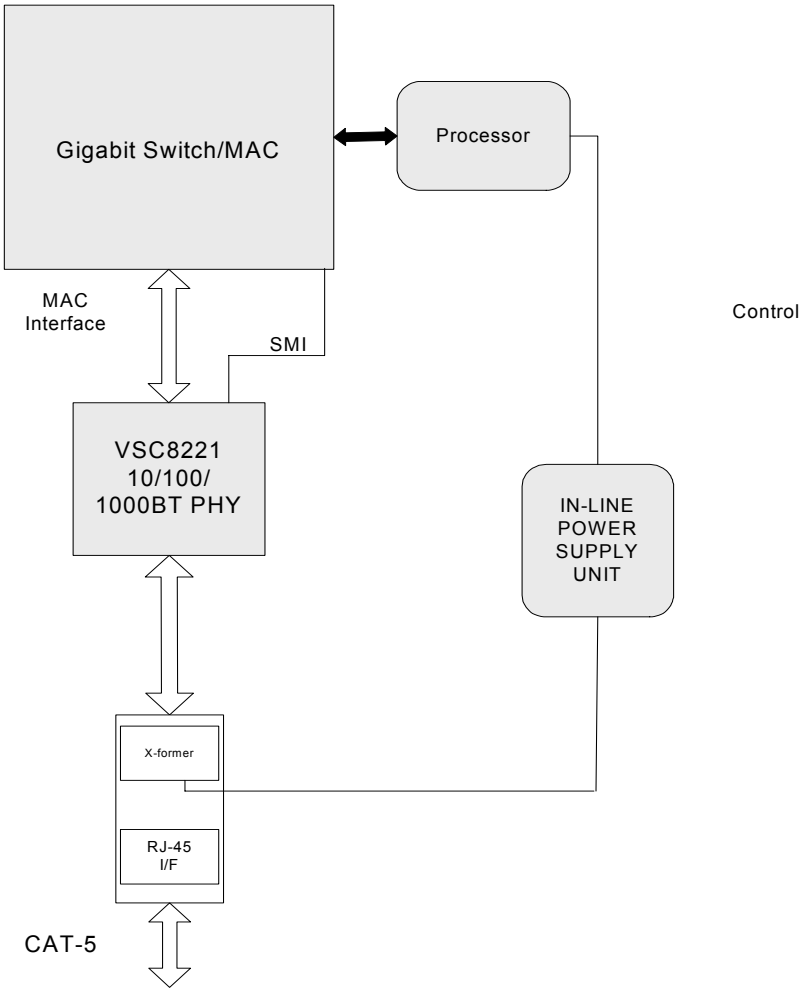


Figure 17. In-line Powered Ethernet Switch Diagram

16.3 In-Line Powered Device Detection (Cisco Method)

This section describes the flow process an Ethernet switch must perform in order to process in-line power requests made by a link partner (LP) capable of receiving in-line power.

1. The in-line powered device detection mode is enabled by setting MII Register bit 23E.10 = 1 and ensuring that the Auto-Negotiation Enable Bit is set (MII Register 0.12 = 1). An interrupt can also be asserted on the $\overline{\text{MDINT}}$ pin when in-line power is needed. This is set by MII Register 25.9 = 1 and ensuring MII Register 25.15 = 1 in order to enable the MDINT pin.
2. The PHY will then start sending a special Fast Link Pulse (FLP) signal to the LP. MII Register 23E.9:8 will equal 00 during the search for devices needing in-line power.
3. The PHY monitors for the special FLP signal looped back by the LP. An LP device capable of receiving in-line power will loopback the special FLP pulses when it is in a powered-down state. This is reported when MII Register 23E.9:8 = 01. If enabled, an interrupt on the $\overline{\text{MDINT}}$ pin will also be asserted. This can be verified as an in-line power detection interrupt by reading MII Register 26.9 = 1, which will subsequently be cleared and the interrupt de-asserted after the read. If an LP device does not loopback the special FLP after a specific time, then MII Register 23E.9:8 = 10.
4. If the PHY reports that the LP needs in-line power, then the Ethernet switch needs to enable in-line power to this port external of the PHY.
5. The PHY automatically disables in-line powered device detection after Event #3 above and now changes to the normal Auto-negotiation process. A link is then auto-negotiated and established when the link status register is set (MII Register bit 1.2 = 1).
6. In a link down event (MII Register bit 1.2 = 0), the in-line power should be disabled to the in-line powered device external of the PHY. The PHY will disable the normal auto-negotiation process and re-enable in-line powered device detection mode.

16.4 IEEE 802.3af (DTE Power via MDI)

The VSC8221 is fully compatible with switch designs used in systems that supply power to DTE (Data Terminal Equipment) by means of a MDI (Media Dependent Interface, or twisted pair cable), as specified by IEEE 802.3af standard (Clause 33).

17 Advanced Test Modes

17.1 Ethernet Packet Generator (EPG)

For system-level debugging and in-system production testing, the VSC8221 includes an Ethernet packet generator. This can be used to isolate problems between the MAC and PHY and between a local PHY and remote link partner. It is intended for use with lab testing equipment or in-system test equipment only, and should not be used when the VSC8221 is connected to a live network.

To use the EPG, it must be enabled by writing a “1” to MII Register 29E.15. This effectively disables all MAC-interface transmit pins and selects the EPG as the source for all data transmitted onto the VSC8221 media interface. For this reason, packet loss will occur if the EPG is enabled during transmission of packets from MAC to PHY. The MAC receive pins will still be active when the EPG is enabled, however. If it is necessary to disable the MAC receive pins as well, this can be done by writing a “1” to MII Register bit 0.10.

When a “1” is written to MII Register Bit 29E.14, the VSC8221 will begin transmitting IEEE802.3 layer-2 compliant packets with a data pattern of repeating 16-bit words as specified in MII Register 30E. The source and destination addresses for each packet, packet size, interpacket gap, FCS state and transmit duration can all be controlled through MII Register 29E. Note that if MII Register Bit 29E.13 is cleared, MII Register Bit 29E.14 will be cleared automatically after 30,000,000 packets have been transmitted.

17.2 CRC Counter

When the EPG is enabled, a bad-CRC counter is also available for all incoming packets. This counter is available in MII Register Bits 23E.7:0 - CRC Counter and is automatically cleared when read.

17.3 Far-End Loopback

Far-end loopback mode, when enabled (MII Register bit 23.3 = 1), forces incoming data from a link partner on the media interface to be retransmitted back to the link partner on the media interface as shown in the figure below. In addition, the incoming data will also appear on the receive data pins (RDP/RDN) of the MAC interface. Data present on the transmit pins of the MAC interface are ignored in this mode. For more information, please refer to MII Register 23 (Extended PHY Control Register #1).

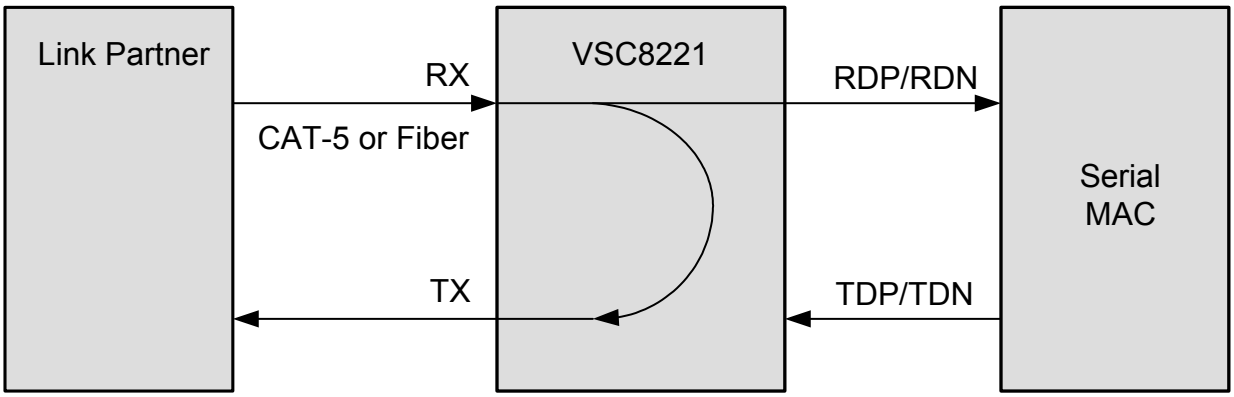


Figure 18. Far-end Loopback Block Diagram

17.4 Near-End Loopback

When Near-end loopback is set (MII Register bit 0.14 = 1), the Transmit Data (TDP/TDN) on the MAC interface is looped back onto the Receive Data (RDP/RDN) pins to the MAC as shown in the figure below. In this mode, the CAT-5 media link is dropped.

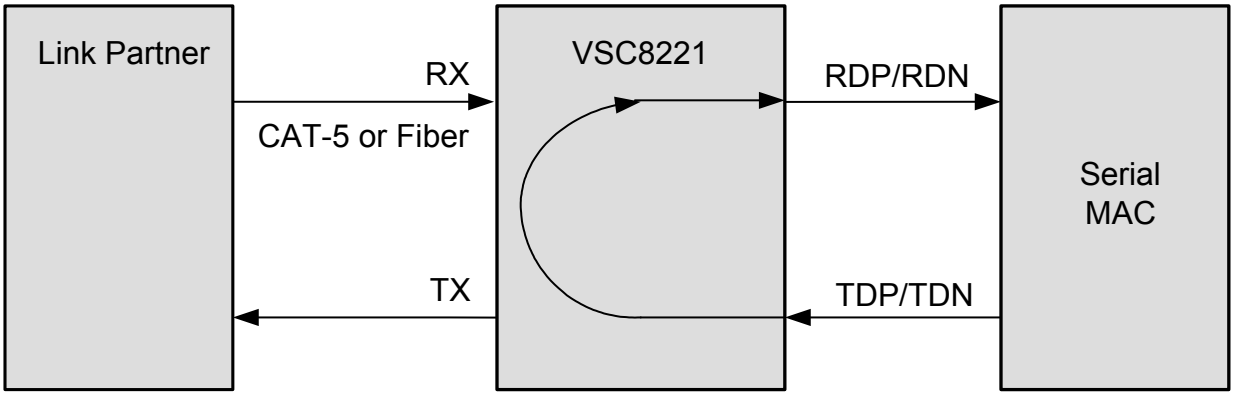


Figure 19. Near-end Loopback Block Diagram

17.5 Connector Loopback

Connector Loopback allows for the twisted pair interface to be looped back externally. In this mode the PHY must be connected to a loopback connector or a loopback cable. For this loopback, pair A should be connected to the corresponding wire of pair B using a 100Ω resistor, and each wire of pair C should be connected to the corresponding wire of pair D using a 100Ω resistor. This loopback will work in all speeds selected for the interface.

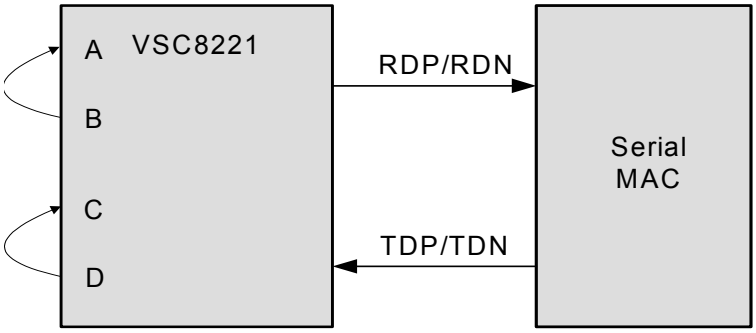


Figure 20. Connector Loopback

The auto-negotiation, speed, and duplex can be configured using MII registers 0,4 and 9. For 1000BT connector loopback only the following additional writes are required in the specific order.

1. Master/Slave configuration forced to Master (MII Register Bits 9.12:11 = 11)

2. Enable 1000BT connector loopback (MII Register 24.0 = 1)

3. Disable pair swap correction (MII Register Bit 18.5=1)

4. Disable auto-negotiation and force 1000BT link (MII Register Bit 0.12=0, MII Register Bit 0.6=1, and MII Register Bit 0.12=0) and force either full or half duplex (MII Register Bit 0.8=0 or 1).

This loopback is also available in the 100BASE-FX mode.

18 HARDWARE CONFIGURATION USING CMODE PINS

Each of the four CMODE pins (CMODE[3:0]) are used to latch a four bit value at PHY reset. A total of sixteen CMODE configuration bits are set at reset. Each CMODE bit represents the default value of a particular PHY register bit and therefore sets a default PHY operating condition at startup.

18.1 Setting the CMODE Configuration Bits

The CMODE bits are set by connecting each CMODE pin to either VDD33A or VSS (ground) through an external 1% resistor. The four bit value latched by the PHY on each CMODE pin depends upon the value of the resistor used to pull-up or pull-down the CMODE pin. CMODE resistor values and connections are defined in the following table:

Table 25. CMODE Pull-up/Pull-down Resistor Values

CMODE bit 3 value	CMODE bit 2 value	CMODE bit 1 value	CMODE bit 0 value	CMODE Resistor Value	Tied to VDD33A or GND
0	0	0	0	0	GND
0	0	0	1	2.26k	GND
0	0	1	0	4.02k	GND
0	0	1	1	5.90k	GND
0	1	0	0	8.25k	GND
0	1	0	1	12.1k	GND
0	1	1	0	16.9k	GND
0	1	1	1	22.6k	GND
1	0	0	0	0	VDD33A
1	0	0	1	2.26k	VDD33A
1	0	1	0	4.02k	VDD33A
1	0	1	1	5.90k	VDD33A
1	1	0	0	8.25k	VDD33A
1	1	0	1	12.1k	VDD33A
1	1	1	0	16.9k	VDD33A
1	1	1	1	22.6k	VDD33A

18.2 CMODE Bit Descriptions

The following table outlines the mapping of each CMODE bit to a PHY operating condition parameter. Each of the PHY operating condition parameters is described in detail in Table 27: "PHY Operating Condition Parameter Description".

Table 26. CMODE Bit to PHY Operating Condition Parameter Mapping

CMODE Pin Name	'CMODE Bit' to 'PHY Operating Condition Parameter' Mapping			
	Bit 3	Bit 2	Bit 1	Bit 0
CMODE0	PHY Address[3]	PHY Address[2]	PHY Address[1]	PHY Address[0]
CMODE1	SFP Mode Disable	PHY Address[4]	SIGDET pin direction	SerDes Line Impedance
CMODE2	PHY Operating Mode[3]	PHY Operating Mode[2]	PHY Operating Mode[1]	PHY Operating Mode[0]
CMODE3	LED Control[1]	SQE Enable	Reserved	Auto-negotiation Advertisement Control[1]

Each of the PHY Operating Condition Parameters mentioned in Table 26 above is described in detail in Table 27.

Table 27. PHY Operating Condition Parameter Description

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
PHY Address[4:0]	CMODE1[2], CMODE0[3:0]	31-0	Sets the PHY Address used to access PHY Registers when the PHY's SMI is in IEEE mode. The value latched is reflected in Extended MII Register 23.15:11.
PHY Operating Mode[3:0]	CMODE2[3:0]	These CMODE bits set the default PHY Operating Mode by setting the default values of MII Register 23.15:12,2:1.	
		0000	802.3z SerDes to CAT5 Media, Clause 37 auto-negotiation auto-sense enabled.
		0100	802.3z SerDes to CAT5 Media, Clause 37 disabled.
		0101	SGMII to CAT5 Media, SCLK enabled.
		1010	802.3z SerDes to CAT5 Media, Media Connector Mode.
		1110	802.3z SerDes to CAT5 Media, Clause 37 enabled.
		1111	SGMII to CAT5 Media, SCLK disabled.
LED Control[1]	CMODE3[3]	This sets the default behavior of LED pins LED[2:0] by setting the startup values of MII Register Bit Register 27 (1Bh) – LED Control Register.	
		0	LED[2:0] = {Link10/Activity, Link100/Activity, Link1000/Activity} (MII Reg 27 = 0000h)
		1	LED[2:0] = {Link/Activity, Link/Activity, Fault} (MII Reg 27 = AA80h)

Table 27. PHY Operating Condition Parameter Description *(continued)*

PHY Operating Condition Parameter Name	CMODE Pin Name and Bit Position	Value	Description
Auto-negotiation Advertisement Control[1]	CMODE3[0]	These CMODE bits set the default auto-negotiation advertisement defaults by setting the defaults of MII Registers 4 and 9.	
		0	10/100/1000BASE-T HDX, FDX
		1	10/100BASE-T HDX, FDX
SFP Mode Disable	CMODE1[3]	This CMODE bit sets the default value of MII Register 21E.15 .	
		0	This sets MII Register 21E.15 = 1. Sets the following PHY defaults: • TXDIS/$\overline{\text{SRESET}}$ is active high i.e. behaves like TXDIS. • MODDEF0/CLKOUT pin functions like MODDEF0 i.e this pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI interface. • RXLOS/SIGDET pins functions like the RXLOS. • The SMI interface is set in MSA mode.
		1	This sets MII Register 21E.15 = 0. Sets the following PHY defaults: • TXDIS/$\overline{\text{SRESET}}$ is active low i.e. behaves like $\overline{\text{SRESET}}$. • MODDEF0/CLKOUT pin functions like CLKOUT i.e this pin drive out a 125Mhz clock. • RXLOS/SIGDET pin functions like the SIGDET. • The SMI interface is set in IEEE mode
SIGDET pin direction	CMODE1[1]	The value of this bit is valid in non-SFP mode when CMODE bit CMODE1[3] is 1. This CMODE bit set the direction of the SIGDET pin by setting the default value of Extended MII Register 19E.1	
		0	Input
		1	Output
SerDes Line Impedance	CMODE1[0]	Sets the internal end termination resistance value of the Serial MAC/ Media Interface Input pins.	
		0	50 Ω
		1	75Ω
SQE Enable	CMODE3[2]	Sets the default value of MII Register 22.12.	
		0	SQE Disabled (MII Register 22.12=1)
		1	SQE Enabled (MII Register 22.12=0)

18.3 Procedure for Selecting CMODE Pin Pull-Up/Pull-Down Resistor Values

1. Using the descriptions in Table 27 column D (“Description”), choose the desired PHY operating condition parameter values from column C (“Value”).
2. Using Table 27 Column B (“CMODE Pin Name and Bit Position”) and the chosen PHY operating condition parameter values, enter the value of each CMODE bit in Table 26: “CMODE Bit to PHY Operating Condition Parameter Mapping”.
3. Choose the value of each CMODE pull-up or pull-down resistor from Table 25: “CMODE Pull-up/Pull-down Resistor Values” based on the CMODE Bit values in Table 26.

19 EEPROM INTERFACE

The EEPROM Interface consists of the EEDAT and EECLK pins of the PHY. If this interface is used, these pins should connect to the SDA and SCL pins respectively of a serial EEPROM that is compatible with the AT24xxx series of ATMEL EEPROMs.

The EEPROM interface on the VSC8221 serves the following purposes:

- It provides the PHY with the ability to self configure its internal registers.
- The system manager can access the EEPROM to obtain information pertaining to the system/module configuration.
- A single EEPROM can be shared among multiple PHYs for their custom configuration.

The PHY detects the EEPROM based on the presence of a pullup on the EEDAT pin. It is initialized using the configuration EEPROM (if present) under the following conditions:

- $\overline{\text{RESET}}$ deassertion.
- TXDIS/$\overline{\text{SRESET}}$ deassertion and Extended MII Register 21E.14 is set.
- S/W reset (MII Register 0.15) is asserted and Extended MII Register 21E.14 is set.

If an EEPROM is present, the start-up control block looks for a “Vitesse Header” (value:16’hBDBD’) at address 0 and 1 of the EEPROM. The address is incremented by 256 until the Vitesse Header is found. If the Vitesse Header is not found, or no EEPROM is connected, the VSC8221 bypasses the EEPROM read step.

Once the Vitesse header is located, the EEPROM Interface block of the PHY searches for its PHY address in bit position 7:3 in the subsequent EEPROM location. Once the PHY address is located, the 11 bit EEPROM address location for the start of the configuration script is read. At this point, the PHY begins reading from this 11 bit EEPROM address and initializes its Register values based on the EEPROM configuration script contents. Refer to Table 28: “Configuration EEPROM Data Format” for details on the configuration EEPROM data format.

The total number of EEPROM bytes needed for a configuration script is equal to:

((Number of Register writes) * 3 + 2 (BDBD) + 2 (PHY address and Configuration Script Address) + 2 (Length of configuration script)).

Data is read from the EEPROM sequentially (at 50 Khz, or 50 kbits/s) until all PHY registers are set. Once all of the PHY registers are set, the PHY enters the ‘NORMAL STATE’. For more information, see Section 20 on page 61.

If the PHY is in the ‘NORMAL STATE’ state, the user can access the EEPROM connected to the EEPROM interface through the SMI. If the SMI is in IEEE mode, the EEPROM can be accessed via the SMI using Extended MII Registers 21E and 22E. If the SMI is in MSA mode, the EEPROM can be accessed directly via the SMI i.e. the PHY behaves as if the MODDEF2 and MODDEEF1 pins of the SMI are directly connected to the EEDAT and EECLK pins of the PHY.[1]

One exception is the memory portion with device/page address ‘110’. This is reserved for the PHY Register access when the PHY’s SMI is set in MSA mode.

If an EEPROM is present, but the EEPROM does not acknowledge (according to the ATMEL EEPROM protocol), the VSC8221 waits for an acknowledgement for approximately 3 seconds. If there is no acknowledgement within 3 seconds, the VSC8221 will abort and continue into normal operation.

19.1 Programming Multiple VSC8221s Using the Same EEPROM

To prevent contention on the 2 wire bus when multiple PHYs use the same EEPROM for initialization, the EEPROM start-up block of each VSC8221 monitors the bus for (PHY Address[4:0] + 1) * 9 + 92 clock cycles for no bus activity and only then attempts to access the EEPROM bus. PhyAddress[4:0] is chosen because these are the PHY Address bits that are unique to each VSC8221 (that is, VSC8221 with lowest PHY Address gets priority in this bus).

[1]EEPROM memory with device address ‘110’ cannot be accessed directly when the SMI is in MSA mode. This device address is reserved for PHY Register access in MSA mode. To access an EEPROM with device address ‘110’ in MSA mode, Extended MII Registers 21E and 22E should be used.

.

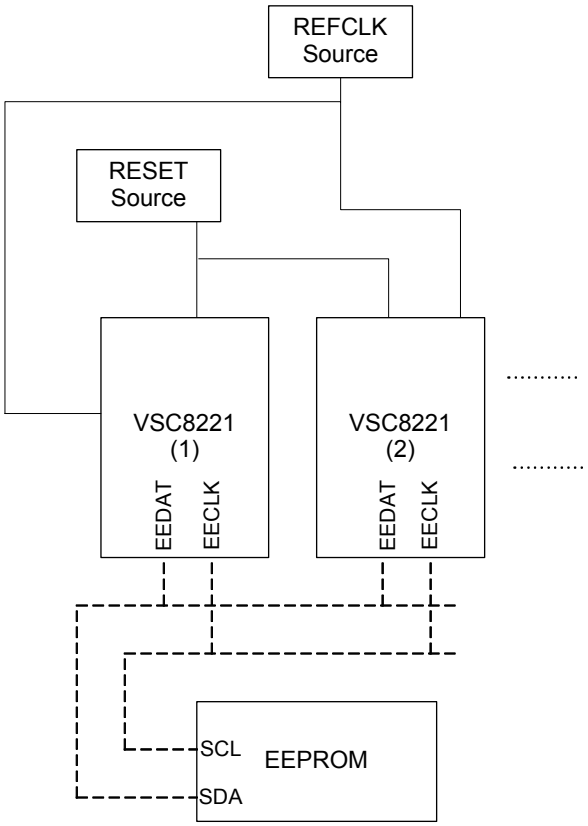


Figure 21. EEPROM Interface Connections

NOTE: The same clock must be used for each VSC8221's REFCLK input. In addition, the $\overline{\text{RESET}}$ pin for each VSC8221 must be driven from the same source to ensure that the reference clock modes within each device are correctly set.

This prevents using the CLKOUT or CLKOUTMICRO output from one VSC8221 to drive the clock input of another VSC8221, if the devices are sharing the same EEPROM.

Table 28. Configuration EEPROM Data Format

Address	Contents
----------	----------
----------	----------
----------	----------
----------	----------
O+7	Data to be written (LSB)
O+6	Data to be written (MSB)
O+5	RegAddress b
O+4	Data to be written (LSB)
O+3	Data to be written (MSB)

Table 28. Configuration EEPROM Data Format *(continued)*

Address	Contents
O+2	RegAddress a
O+1	Number of PHY Register writes *3[7:0]
{bpage_addr3,s_addr3} = O	Number of PHY Register writes *3[15:8]
----------	----------
----------	----------
----------	----------
----------	----------
M+7	Data to be written (LSB)
M+6	Data to be written (MSB)
M+5	RegAddress b
M+4	Data to be written (LSB)
M+3	Data to be written (MSB)
M+2	RegAddress a
M+1	Number of PHY Register writes *3[7:0]
{bpage_addr2,s_addr2} = M	Number of PHY Register writes *3[15:8]
----------	----------
N+7	Data to be written (LSB)
N+6	Data to be written (MSB)
N+5	RegAddress b
N+4	Data to be written (LSB)
N+3	Data to be written (MSB)
N+2	RegAddress a
N+1	Number of PHY Register writes *3[7:0]
{bpage_addr1,s_addr1} = N	Number of PHY Register writes *3[15:8]
----------	----------
7,263,519,..	Starting address for initializing PHY3 s_addr3
6,262,518,..	{PHY Address 1[4:0], 3’bpage_addr3}
5,261,517,..	Starting address for initializing PHY2 s_addr2
4,260,516,..	{PHY Address 2[4:0], 3’bpage_addr2}
3,259,515,..	Starting address for initializing PHY1 s_addr1

Table 28. Configuration EEPROM Data Format *(continued)*

Address	Contents
2,258,514,..	{PHY Address 1[4:0], 3'bpage_addr1}
1,257,513..	8'hBD
0,256,512...	8'hBD

Using the EEPROM Data Format of Table 28 enables multiple PHYs to be initialized in a similar way by reading the same locations from the EEPROM. If the PHYs have to be initialized differently, then the 'Address pointers' will differ for each PHY, along with different PHY configuration data values.

20 PHY STARTUP AND INITIALIZATION

The PHY Startup and Initialization sequence is detailed in the flowchart below.

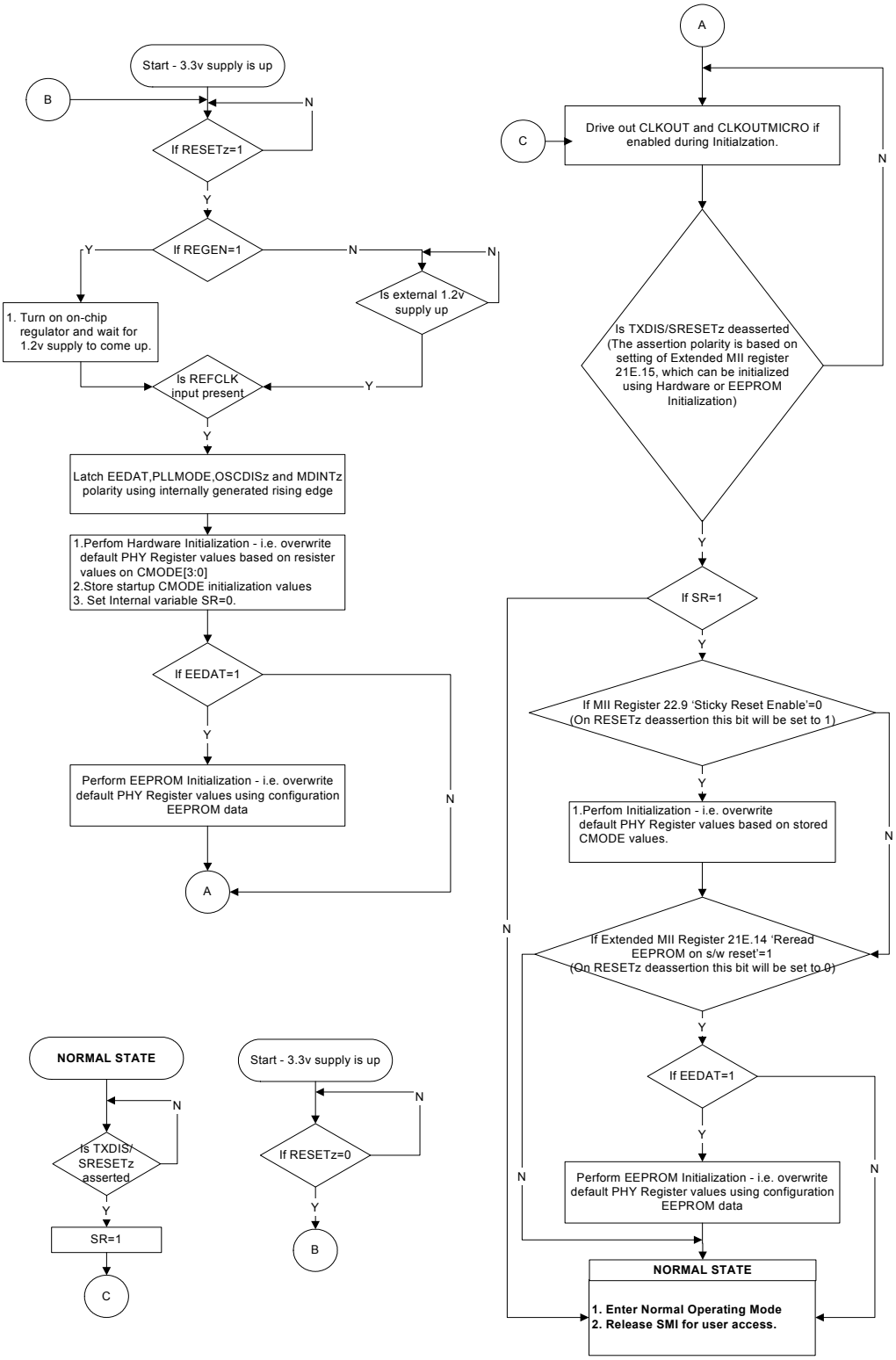


Figure 22. PHY Startup and Initialization Sequence

21 PHY Operating Modes

The PHY Operating Mode is set according to the value of MII Register 23.15:12,23.2:1. For more information, see Section 18 on page 53 and Section 19 on page 57 for details on PHY Operating Mode configuration at startup. The following table summarizes the PHY operating modes.

Table 29. PHY Operating Modes

Operating Mode Category	MII Register 23.15:12, 23.2:1	CMODE2 [3:0]	MAC Interface	Media Interface	Other Settings
Serial MAC PHY Operating Modes	1111, 00	0100	802.3z Ser-Des	CAT5	Clause 37 disabled
	1110, 01	1110	802.3z Ser-Des	CAT5	Clause 37 enabled
	1110, 10	1010	802.3z Ser-Des	CAT5	Clause 37 enabled, Media Convertor Mode
	1110, 00	0000	802.3z Ser-Des	CAT5	With Clause 37 Auto-Negotiation Detection
	1010, 01	1111	SGMII	CAT5	625Mhz SCLK Clock Disabled
	1000, 01	0101	SGMII	CAT5	625MHz SCLK Clock Enabled
	1001, 00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Enabled
	1011, 00		SGMII	CAT5	Modified Clause 37 auto-negotiation disabled, 625MHz SCLK Clock Disabled

Note: For more information about VSC8221 operating modes, see *Designing a Copper SFP using the VSC8221* application note available on the Vitesse Web site.

22 PHY Register Set Conventions

The user can control the PHY's features, operating modes, etc. by setting the PHY Registers to the desired values. The PHY provides access to its Registers using the Serial Management Interface. For details on PHY Register access, refer to Section 12 on page 33.

22.1 PHY Register Set Structure

The register access protocol, as defined by the IEEE 802.3 specification, reserves 5 bits for register addressing. This limits the register space to 32, 16 bit wide registers. Of these, registers addressed 0 through 15 are defined by the IEEE 802.3 specification and registers addressed 16 through 31 are vendor specific. To provide extensive feature control of the PHY, the vendor specific registers addressed 16 through 31 have been divided into two Page views, called PAGE0 and PAGE1, enabling access to 32 vendor specific registers instead of 16.

PAGE0 is the default page view. To switch to PAGE1 write 0001 to PHY Register 31. To switch to PAGE0 write 0000h to PHY Register 31.

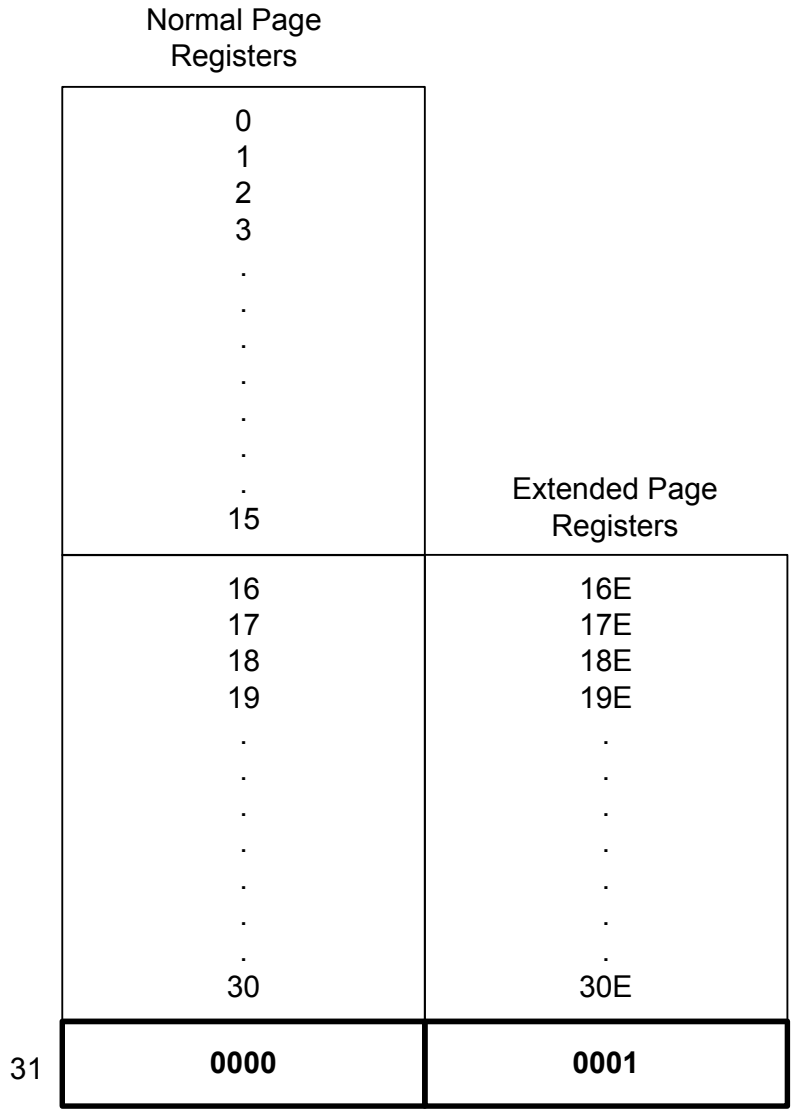


Figure 23. Extended Page Register Diagram

22.2 PHY Register Set Nomenclature

Table 30. Register Set Nomenclature

Register Address	Page View	Naming Convention
0-15	- NA-	MII Register
16-31	PAGE0	MII Register
16-31	PAGE1	Extended Page MII Register (Referred to with an 'E' after the register number e.g. 20E.15 is Page 1 Register 20 bit 15)

22.3 PHY Register Bit types

PHY Register bit types are defined in the table below:

Table 31. PHY Register Bit Types

Register Bit Type	Description
R/W	Read and Write, effective immediately
RO	Read Only (must be written '0', unless specified otherwise)
RO SC	Read Only, Self Clears after Read
LH	Latched High, Clears after Read
LL	Latched Low, Clears after Read
SC	Self-Cleared
RWSW	Read and Write, effective after s/w reset. This register will read the new value only after s/w reset.

"Sticky" refers to the behavior of the register bit(s) after a software reset. If an "S" appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, as long as MII Register bit 22.9 - Sticky Reset Enable is set.

If an "SS" appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, regardless of the state of MII Register bit 22.9 - Sticky Reset Enable.

23 PHY Register Set

23.1 PHY Register Names and Addresses

Table 32. PHY Register Names and Addresses

Register Name	Register Number	Register Address (hex)
Mode Control	0	00
Mode Status	1	01
PHY Identifier Register # 1	2	02
PHY Identifier Register # 2	3	03
Auto-Negotiation Advertisement	4	04
Auto-Negotiation Link Partner Ability	5	05
Auto-Negotiation Expansion	6	06
Auto-Negotiation Next-Page Transmit	7	07
Auto-Negotiation Link Partner Next Page Receive	8	08
1000BASE-T Control	9	09
1000BASE-T Status Register # 1	10	0A
Reserved	11	0B
Reserved	12	0C
Reserved	13	0D
Reserved	14	0E
1000BASE-T Status Register #2	15	0F
Reserved	16	10
Reserved	17	11
Bypass Control	18	12
Reserved	19	13
Reserved	20	14
Reserved	21	15
Control & Status	22	16
PHY Control # 1	23	17
PHY Control # 2	24	18
Interrupt Mask	25	19
Interrupt Status	26	1A
LED Control	27	1B
Auxiliary Control & Status	28	1C

Table 32. PHY Register Names and Addresses *(continued)*

Register Name	Register Number	Register Address (hex)
Reserved	29	1D
MAC Interface Clause 37 Auto-negotiation Control & Status	30	1E
Extended Page Access	31	1F
Reserved	16E	10
SerDes Control #2	17E	11
Reserved	18E	12
SerDes Control Register # 2	19E	13
Extended PHY Control # 3	20E	14
EEPROM Interface Status and Control	21E	15
EEPROM Data Read/Write	22E	16
Extended PHY Control # 4	23E	17
Reserved	24E	18
Reserved	25E	19
Reserved	26E	1A
Reserved	27E	1B
Reserved	28E	1C
1000BASE-T Ethernet Packet Generator (EPG) # 1	29E	1D
1000BASE-T Ethernet Packet Generator (EPG) # 2	30E	1E

23.2 MII Register Descriptions

23.2.1 Register 0 (00h) – Mode Control Register

Register 0 (00h) – Mode Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Software Reset[1]	R/W SC	1 = Reset asserted 0 = Reset de-asserted	0	
14	Near End Loopback	R/W	1 = Loopback on 0 = Loopback off	0	
6, 13	Forced Speed Selection	R/W	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	10	
12	Auto-Negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	1	
11	Power-Down[2]	R/W	1 = Power-down 0 = Power-up	0	
10	Isolate	R/W	1 = Disable MAC outputs 0 = Normal Operation	0	
9	Restart Auto-Negotiation	R/W SC	1 = Restart MII 0 = Normal operation	0	
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0	
7	Reserved	RO		0	
6	MSB for Speed Selection (see bit 13 above)		See “Forced Speed Selection” Above	1	
5:0	Reserved			000000	

[1] In MSA mode, when this bit is set, the PHY does not return the correct values for the subsequent register read operations. In order to read the correct PHY register values, the station manager must provide 70 clock cycles on the MODDEF1/MDC pin or perform two byte read operations on any eeprom address other than in page ‘110’ immediately following s/w reset.

[2] The status of the Link Status bit, MII Register 1.2, remains unchanged when this bit is set.

0.15 – Software Reset

Writing a “1” to bit 0.15 initiates a software reset. Once Software Reset is asserted, the PHY is returned to normal operating mode and is ready for the next SMI transaction, so Software Reset always reads back “0”. Software Reset restores all SMI registers to their default states, except for registers marked with an “S” or “SS” in the sticky column.

0.14 – Near End Loopback

When Near End Loopback is asserted, the Transmit Data (TXD) on the MAC interface is looped back as Receive Data (RXD). In loopback mode, no signal is transmitted over the network media. The loopback mechanism works in all (10/100/1000) modes of operation. The operating mode is determined by bits 0.13 and 0.6 (forced speed selection).

0.13, 0.6 – Forced Speed Selection

These bits determine the 10/100/1000 speed when auto-negotiation is disabled by clearing control bit 0.12. These bits are ignored if control bit 0.12 is set. These bits also determine the operating mode when Near End Loopback (0.14) is set to “1”.

0.12 – Auto-Negotiation Enable

After a power-up or reset, the PHY automatically activates the auto-negotiation state machine, setting bit 0.12 to a “1”. If a “0” is written to bit 0.12, the auto-negotiation process is disabled and the present contents of the PHY’s SMI register bits determine the operating characteristics. Note that auto-negotiation is always required in 1000BASE-T mode.

0.11 – Power-Down

Power-Down functions the same as Software Reset, except that it is not self-clearing, and that R/W SMI bits are *not* restored to their default states by Power-Down. The RGMII pins (except for SMI pins MDC, MDIO, and MDINT#) are electrically isolated during power-down. After Power-Down is released (i.e., set to “0”), the PHY will be ready for normal operation before the next SMI transaction. If auto-negotiation is enabled, the PHY will begin auto-negotiation immediately upon exiting Power-Down.

0.10 – Isolate[1]

When Isolate is asserted (i.e., set to “1”), all Serial MAC outputs (except for MDIO) will be high impedance. Operation of the PHY is otherwise unaffected. For example, if Isolate is asserted while CAT5 auto-negotiation is under way, auto-negotiation will continue unaffected.

0.9 – Restart Auto-Negotiation

When restart auto-negotiation is asserted (i.e., set to “1”), the auto-negotiation state machine will restart the auto-negotiation process, even if it is in the midst of an auto-negotiation process. This control bit is self-clearing, meaning that it will always return a “0” when read.

0.8 – Duplex Mode

Bit 0.8 determines the duplex mode of the VSC8221 when auto-negotiation is disabled. Changes to the state of Duplex Mode while auto-negotiation is enabled are ignored.

0.7 – Reserved

0.5:0 – Reserved

[1]When set, while the PHY’s SerDes side auto-negotiation function is enabled, the PHY will drop the CAT5 link. Also, setting of this bit does not disable the output clock on the SCLKP and SCLKN pins.

23.2.2 Register 1 (01h) – Mode Status Register

Register 1 (01h) – Mode Status Register

Bit	Name	Access	States	Reset Value	Sticky
15	100BASE-T4 Capability	RO	1 = 100BASE-T4 capable	0	
14	100BASE-X FDX Capability	RO	1 = 100BASE-X FDX capable	1	
13	100BASE-X HDX Capability	RO	1 = 100BASE-X HDX capable	1	
12	10BASE-T FDX Capability	RO	1 = 10BASE-T FDX capable	1	
11	10BASE-T HDX Capability	RO	1 = 10BASE-T HDX capable	1	
10	100BASE-T2 FDX Capability	RO	1 = 100BASE-T2 FDX capable	0	
9	100BASE-T2 HDX Capability	RO	1 = 100BASE-T2 HDX capable	0	
8	Extended Status Enable	RO	1 = Extended status information present in R15	1	
7	Reserved	RO		0	
6	Preamble Suppression Capability	RO	1 = MF preamble may be suppressed 0 = MF preamble always required	1	
5	Auto-Negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation not complete	0	
4	Remote Fault	RO LH	1 = Far-end fault detected 0 = No fault detected	0	
3	Auto-Negotiation Capability	RO	1 = Auto-negotiation capable	1	
2	Link Status[1]	RO LL	1 = Link is up 0 = Link is down	0	
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0	
0	Extended Capability	RO	1 = Extended register capable	1	

[1] The status of this bit remains unchanged when the PHY is put in Power Down mode by setting MII Register 0.11 or by asserting the TXDIS/$\overline{\text{SRESET}}$ pin.

1.15 – 100BASE-T4 Capability

The VSC8221 is not 100BASE-T4 capable, so this bit is hard-wired to “0”.

1.14 – 100BASE-X FDX Capability

The VSC8221 is 100BASE-X FDX capable, so this bit is hard-wired to “1”.

1.13 – 100BASE-X HDX Capability

The VSC8221 is 100BASE-X HDX capable, so this bit is hard-wired to “1”.

1.12 – 10BASE-T FDX Capability

The VSC8221 is 10BASE-T FDX capable, so this bit is hard-wired to “1”.

1.11 – 10BASE-T HDX Capability

The VSC8221 is 10BASE-T HDX capable, so this bit is hard-wired to “1”.

1.10 – 100BASE-T2 FDX Capability

The VSC8221 is not 100BASE-T2 FDX capable, so this bit is hard-wired to “0”.

1.9 – 100BASE-T2 HDX Capability

The VSC8221 is not 100BASE-T2 HDX capable, so this bit is hard-wired to “0”.

1.8 – Extended Status Enable

The VSC8221 is extended status capable, so this bit is hard-wired to “1”.

1.7 – Reserved

1.6 – Preamble Suppression Capability

The VSC8221 accepts management frames on the SMI without preambles, so preamble suppression capability is hard-wired to “1”. The management frame preamble may be as short as 1 bit.

1.5 – Auto-Negotiation Complete

When this bit is a “1”, the contents of Registers 4, 5, 6, 10 and 28 are valid.

1.4 – Remote Fault

Bit 1.4 will be set to “1” if the Link Partner signals a far-end fault. The bit is cleared automatically upon a read if the far-end fault condition has been removed.

1.3 – Auto-Negotiation Capability

The VSC8221 is auto-negotiation capable, so this bit is hard-wired to “1”. Note that this bit will read a “1” even if auto-negotiation is disabled via bit 0.12.

1.2 – Link Status

This bit will return a “1” when the VSC8221 link state machine has reached the “link pass” state, meaning that a valid link has been established. If the link is subsequently lost, the Link Status will revert to a “0” state. It will remain a “0” until Link Status is read while the link state machine is in the “link pass” state.

1.1 – Jabber Detect

Note that Jabber Detect is required for 10BASE-T mode only. Jabber Detect will be set to “1” when the jabber condition is detected. Jabber Detect will be cleared automatically when this register is read.

1.0 – Extended Capability

The VSC8221 has extended register capability, so this bit is hard-wired to “1”.

23.2.3 Register 2 (02h) – PHY Identifier Register #1

	Register 2 (02h) – PHY Identifier Register #1				
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Organizationally Unique Identifier	RO	OUI most significant bits (Vitesse OUI bits 3:18)	0000000000001111 or (000Fh)	

2.15:0 – PHY Identifier Register #1

Vitesse has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 3 to 18 are used in this register.

23.2.4 Register 3 (03h) – PHY Identifier Register #2

Register 3 (03h) – PHY Identifier Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:10	Organizationally Unique Identifier	RO	OUI least significant bits (Vitesse OUI bits 19:24)	110001	
9:4	Vendor Model Number	RO	Vendor's model number (IC)	010101 = VSC8221	
3:0	Vendor Revision Number	RO	Vendor's revision number (IC)	0001 = Silicon Revision C	

3.15:10 – OUI

Vitesse has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 19 to 24 are used in this register.

3.9:4 - Vendor Model Number

The Model no. of this IC is '010101'.

3.3:0 - Vendor Revision Number

The current Revision Number of this IC is '0001'.

23.2.5 Register 4 (04h) – Auto-Negotiation Advertisement Register

Register 4 (04h) – Auto-Negotiation Advertisement Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0	
14	Reserved	RO		0	
13	Transmit Remote Fault	R/W	1 = Transmit remote fault	0	
12	Reserved	RO		0	
11	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	CMODE	
10	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	CMODE	
9	Advertise 100BASE-T4 Capability	R/W	1 = 100BASE-T4 capable	0	
8	Advertise 100BASE-TX FDX	R/W	1 = 100BASE-TX FDX capable	CMODE	
7	Advertise 100BASE-TX HDX	R/W	1 = 100BASE-TX HDX capable	CMODE	
6	Advertise 10BASE-T FDX	R/W	1 = 10BASE-T FDX capable	CMODE	
5	Advertise 10BASE-T HDX	R/W	1 = 10BASE-T HDX capable	CMODE	
4:0	Advertise Selector Field	R/W		00001	

This register controls the advertised abilities of the local (not remote) PHY. The state of this register is latched when the auto-negotiation state machine enters the ABILITY_DETECT state. Thus, any writes to this register prior to completion of auto-negotiation as indicated by MII Register bit 1.5 should be followed by a re-negotiation for the new values to be properly used for auto-negotiation. Once auto-negotiation has completed, this register value may be read via the SMI to determine the highest common denominator technology.

4.15 – Auto-Negotiation Additional Next-Page Transmission Request

The VSC8221 supports additional Next-Page transmission through MII Register bit 4.15. See description of MII Register bit 18.1 for more details on Next-Page exchanges.

4.14, 4.12 – Reserved

4.13 – Transmit Remote Fault

This bit is used by the local MAC to communicate a fault condition to the link partner during auto-negotiation. This bit does not have any effect on the local PHY operation. This bit is automatically cleared following a successful negotiation with the Link Partner. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This discrepancy is handled in MII Extended register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR.

4.11 – Advertise Asymmetric Pause Capability

This bit is used by the local MAC to communicate Asymmetric Pause Capability to the link partner during auto-negotiation. This has no effect on PHY operation. Changing this bit in Clause-28 view will also change bit 4.8 in Clause-37 view.

4.10 – Advertise Symmetric Pause Capability

This bit is used by the local MAC to communicate Symmetric Pause Capability to the link partner during auto-negotiation. This has no effect on PHY operation. Changing this bit in Clause-28 view will also change bit 4.9 in Clause-37 view.

4.9:5 – Advertise Capability

Bits 4.9:5 allow the user to customize the ability information transmitted to the Link Partner during auto-negotiation. By writing a “1” to any of these bits, the corresponding ability will be advertised to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. The state of these bits has no other effect on the operation of the local PHY. Resetting the chip restores the default bit values. Note that the default values of these bits indicate the true ability of the VSC8221. These bits are not available for read or write in Clause-37 view.

4.4:0 – Advertise Selector Field

Since the VSC8221 is a member of the 802.3 class of PHYs, the Advertise Selector Field defaults to “00001”. These bits are R/W because the Ethernet standard requires them to be R/W. Changing the value of these bits has no effect on PHY operation.

23.2.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Bit	Name	Access	States	Reset Value	Sticky
15	LP Next-Page Transmit Request	RO	1 = LP NP transmit request	0	
14	LP Acknowledge	RO	1 = LP acknowledge	0	
13	LP Remote Fault	RO	1 = LP remote fault	0	
12	Reserved	RO		0	
11	LP Asymmetric Pause Capability	RO	1 = LP Advertise Asymmetric Pause capable	0	
10	LP Symmetric Pause Capability	RO	1 = LP Advertise Symmetric Pause capable	0	
9	LP Advertise 100BASE-T4 Capability	RO	1 = LP Advertise 100BASE-T4 capable	0	
8	LP Advertise 100BASE-TX FDX	RO	1 = LP 100BASE-TX FDX capable	0	
7	LP Advertise 100BASE-TX HDX	RO	1 = LP 100BASE-TX HDX capable	0	
6	LP Advertise 10BASE-T FDX	RO	1 = LP 10BASE-T FDX capable	0	
5	LP Advertise 100BASE-T HDX	RO	1 = LP 100BASE-T HDX capable	0	
4:0	LP Advertise Selector Field	RO	LP Advertise Selector Field	00000	

5.15 – LP Next-Page Transmit Request

Bit 5.15 returns a “1” when the Link Partner implements the Next-Page function and has Next-Page information it wants to transmit. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

5.14 – LP Acknowledge

Bit 5.14 returns a “1” when the Link Partner signals that it has successfully received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

5.13 – LP Remote Fault

Bit 5.13 returns a “1” when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use this bit. Note that IEEE Clause-37 provides for two remote fault bits, while Clause-28 provides only a single remote fault bit. This difference is handled in Extended MII register bits 16E.2:1 - Remote Fault Mapping Mask and 16E.0 - Remote Fault Mapping OR. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.12 – Reserved

5.11 – LP Asymmetric Pause Capability

The LP Asymmetric Pause Capability bit indicates whether the Link Partner has asymmetric pause capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.10 – LP Symmetric Pause Capability

The LP Symmetric Pause Capability bit indicates whether the Link Partner supports symmetric pause frame capability. This bit is used by the Link Partner’s MAC to communicate symmetric pause capability to the local MAC. It has no effect on PHY operation. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.9:5 – LP Advertise Capability

Bits 5.9:5 reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner advertises capability of performing the corresponding mode of operation. These bits are not available for read in Clause-37 view, but remain valid for CAT-5 copper media and can be viewed by switching to Clause-28 view.

5.4:0 – LP Advertise Selector Field

Bits 5.4:0 indicate the state of the Link Partner’s Selector Field. The local PHY does not otherwise use these bits.

23.2.7 Register 6 (06h) – Auto-Negotiation Expansion Register

Register 6 (06h) – Auto-Negotiation Expansion Register

Bit	Name	Access	States	Reset Value	Sticky
15:5	Reserved	RO		00000000000	
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault	0	
3	LP Next-Page Able	RO	1 = LP Next-Page capable	0	
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	1	
1	Page Received	RO LH	1 = New page has been received	0	
0	LP Auto-Negotiation Able	RO	1 = LP auto-negotiation capable	0	

6.15:5 – Reserved

6.4 – Parallel Detection Fault

Parallel Detection Fault returns a “1” when a parallel detection fault occurs in the local auto-negotiation state machine. Once set, this bit is automatically cleared when (and only when) Register 6 is read.

6.3 – LP Next-Page Able

LP Next-Page Able returns a “1” when the Link Partner has Next-Page capabilities. This bit is used in the auto-negotiation state machines, as defined in Clause 28 of IEEE 802.3. The state of this bit is valid when either the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

6.2 – Local PHY Next-Page Able

Since the VSC8221 is next-page capable during Clause-28 auto-negotiation, this bit is hard-wired to “1”.

6.1 – Page Received

Page Received is set to “1” when a new Link Code Word is received from the Link Partner, validated, and acknowledged. Page Received is automatically cleared when (and only when) Register 6 is read via the SMI.

6.0 – LP Auto-Negotiation Able

LP Auto-Negotiation Able is set to “1” if the Link Partner advertises auto-negotiation capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

23.2.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register

Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register

Bit	Name	Access	States	Reset Value	Sticky
15	Next Page	R/W	1 = More pages follow 0 = Last page	0	
14	Reserved	RO		0	
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1	
12	Acknowledge2	R/W	1 = Will comply with request 0 = Cannot comply with request	0	
11	Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0	
10:0	Message/Unformatted Code	R/W		00000000001	

7.15 – Next Page

The Next Page bit indicates whether this is the last Next-Page to be transmitted. By default, this bit is set to “0”, indicating that this is the last page.

7.14 – Reserved

7.13 – Message Page

The Message Page bit indicates whether this page is a message page or an unformatted page. This bit does not otherwise affect the operation of the local PHY. By default, this bit is set to “1”, indicating that this is a message page.

7.12 – Acknowledge2

The Acknowledge2 bit indicates if the local MAC reports that it is able to act on the information (or perform the task) indicated in the previous message. The local PHY does not interpret or act on changes in the state of this bit.

7.11 – Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. The Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word.

7.10:0 – Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner. The local PHY passes the message code to the Link Partner without interpreting or reacting to it. By default, this code is set to “000 0000 0001”, indicating a null message.

23.2.9 Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register

Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register

Bit	Name	Access	States	Reset Value	Sticky
15	LP Next Page	RO	1 = More pages follow 0 = Last page	0	
14	LP Acknowledge	RO	1 = LP acknowledge	0	
13	LP Message Page	RO	1 = Message page 0 = Unformatted page	0	
12	LP Acknowledge2	RO	1 = LP will comply with request	0	
11	LP Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0	
10:0	LP Message/Unformatted Code	RO		00000000000	

SMI Register 8 contains the Link Partner’s Next-Page register contents. The contents of this register are only valid when the Page Received bit (6.1) is set.

8.15 – LP Next Page

This bit indicates if more pages follow from the Link Partner.

8.14 – LP Acknowledge

This bit returns a “1” when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

8.13 – LP Message Page

The Message Page bit indicates if the page received from the Link Partner is a message page or an unformatted page.

8.12 – LP Acknowledge2

The Acknowledge2 bit indicates whether the Link Partner MAC reports that it is able to act on the information (or perform the task) indicated in the message. The local PHY does not interpret or act on changes in the state of this bit.

8.11 – LP Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. In the Link Partner, the Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word from the Link Partner.

8.10:0 – LP Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted by the Link Partner.

23.2.10 Register 9 (09h) – 1000BASE-T Control Register

Register 9 (09h) – 1000BASE-T Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:13	Transmitter Test Mode	R/W	Described below, per IEEE 802.3, 40.6.1.1.2	000	
12	MASTER/SLAVE Manual Configuration Enable	R/W	1 = Enable MASTER/SLAVE Manual Configuration value 0 = Disable MASTER/SLAVE Manual Configuration value	0	
11	MASTER/SLAVE Manual Configuration Value	R/W	1 = Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.	0	
10	Port Type	R/W	1 = Multi-port device 0 = Single-port device	0	
9	1000BASE-T FDX Capability	R/W	1 = PHY is 1000BASE-T FDX capable	CMODE	
8	1000BASE-T HDX Capability	R/W	1 = PHY is 1000BASE-T HDX capable	CMODE	
7:0	Reserved	R/W		00000000	

9.15:13 – Transmitter/Receiver Test Mode[1]

This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information.

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

[1]The state of this register is internally latched when the auto-negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in SLAVE timing mode.
- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:
  The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in the following table. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

9.12 – MASTER/SLAVE Manual Configuration Enable[1]

When this bit is set to “0” (default), the MASTER/SLAVE designation of the local PHY is determined using the arbitration protocol established in the IEEE Ethernet standard. When this bit is set to “1”, the MASTER/SLAVE designation of the local PHY is set by bit 9.11. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.11 – MASTER/SLAVE Configuration Value[1]

This bit is ignored when bit 9.12 is set to “0”. However, if bit 9.12 is set to “1”, bit 9.11 determines the MASTER/SLAVE designation of the local PHY. If bit 9.12 is set to “1” and bit 9.11 set to “0” (default), the local PHY is forced to be a SLAVE. If bit 9.12 is set to “1” and bit 9.11 set to “1”, the local PHY is forced to be a MASTER. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.10 – Port Type[1]

Since the VSC8221 is a single port physical layer transceiver, bit 9.10 is set to “0” by default. When set to “0”, this bit indicates a preference for operation as a SLAVE. If the Link Partner does not indicate the same preference, the local PHY will operate as a SLAVE, and the Link Partner will be a MASTER. Otherwise, the normal MASTER/SLAVE assignment protocol is used.

[1]The state of this register is internally latched when the auto-negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

9.9 – 1000BASE-T FDX[1]

Since the VSC8221 is 1000BASE-T FDX capable, this bit is “1” by default. If bit 9.9 is written to be “0”, the auto-negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T FDX. Note that the Link Partner will be notified of the state of bit 9.9 during auto-negotiation. After auto-negotiation is complete, changing the state of this bit has no effect unless auto-negotiation is manually restarted.

9.8 – 1000BASE-T HDX[1]

Since the VSC8221 is 1000BASE-T HDX capable, this bit is “1” by default. If bit 9.8 is written to be “0”, the auto-negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T HDX. Note that the Link Partner will be notified of the state of bit 9.8 during auto-negotiation. After auto-negotiation is complete, changing the state of this bit has no effect unless auto-negotiation is manually restarted.

9.7:0 – Reserved

23.2.11 Register 10 (0Ah) – 1000BASE-T Status Register #1

Register 10 (0Ah) – 1000BASE-T Status Register #1

Bit	Name	Access	States	Reset Value	Sticky
15	MASTER/SLAVE Configuration Fault	RO LH SC	1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected	0	
14	MASTER/SLAVE Configuration Resolution	RO	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	1	
13	Local Receiver Status	RO	1 = Local receiver OK (loc_rcvr_status == OK) 0 = Local receiver not OK (loc_rcvr_status == NOT_OK)	0	
12	Remote Receiver Status	RO	1 = Remote receiver OK (rem_rcvr_status == OK) 0 = Remote receiver not OK (rem_rcvr_status == NOT_OK)	0	
11	LP 1000BASE-T FDX Capability	RO	1 = LP 1000BASE-T FDX capable 0 = LP not 1000BASE-T FDX capable	0	
10	LP 1000BASE-T HDX Capability	RO	1 = LP is 1000BASE-T HDX capable 0 = LP is not 1000BASE-T HDX capable	0	
9:8	Reserved	RO		00	
7:0	Idle Error Count	RO SC		00000000	

10.15 – MASTER/SLAVE Configuration Fault[2]

This bit indicates whether a MASTER/SLAVE configuration fault has been detected by the local PHY. A configuration fault occurs if both the local and remote PHYs are forced to the same MASTER/SLAVE state, or if no resolution is reached after seven retries. When such a fault has been detected, this bit is set to “1”, but the PHY continues to renegotiate until the MASTER/SLAVE configuration is resolved. Once set, this bit is automatically cleared when (and only when) Register 10 is read via the SMI.

[1]The state of this register is internally latched when the auto-negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

[2]This bit is valid only when the Page Received bit (6.1) is set to a “1” and if MII Register bit 9.9 or 9.8 is set.

10.14 – MASTER/SLAVE Configuration Resolution[1]

By default, the MASTER/SLAVE configuration is determined as part of the auto-negotiation process. However, the MASTER/SLAVE status can optionally be manually forced via bits in MII Register 9. Bit 10.14 indicates the final MASTER/SLAVE configuration status for the local PHY. This bit can change state only as a result of the reset or subsequent restart of the auto-negotiation process. This bit is only valid when the Auto-Negotiation Complete bit (1.5) is set.

10.13 – Local Receiver Status[1]

Bit 10.13 indicates the state of the loc_rcvr_status flag within the PMA receive function within the local PHY.

10.12 – Remote Receiver Status[1]

Bit 10.12 indicates the state of the rem_rcvr_status flag within the PMA receive function within the local PHY.

10.11 – LP 1000BASE-T FDX Capability[1]

Bit 10.11 is set to “1” if the Link Partner PHY advertises 1000BASE-T FDX capability. Otherwise, this bit is set to “0”. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

10.10 – LP 1000BASE-T HDX Capability[1]

Bit 10.10 is set to “1” if the Link Partner PHY advertises 1000BASE-T HDX capability. Otherwise, this bit is set to “0”. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

10.9:8 – Reserved

10.7:0 – Idle Error Count[1]

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both the local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rx_error_status in the PMA receive function is equal to ERROR. Bits 10.7:0 are reset to all “0”s when the error count is read by the management function, or upon execution of the PCS reset function, and they are saturated to all “1”s in case of overflow.

23.2.12 Register 11 (0Bh) – Reserved Register

Register 11 (0Bh) – Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

11.15:0 – Reserved

[1]This bit is valid only when the Page Received bit (6.1) is set to a “1” and if MII Register bit 9.9 or 9.8 is set.

23.2.13 Register 12 (0Ch) – Reserved Register

Register 12 (0Ch) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

12.15:0 – Reserved

23.2.14 Register 13 (0Dh) – Reserved Register

Register 13 (0Dh) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

13.15:0 – Reserved

23.2.15 Register 14 (0Eh) – Reserved Register

Register 14 (0Eh) – Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

14.15:0 – Reserved

23.2.16 Register 15 (0Fh) – 1000BASE-T Status Register #2

Register 15 (0Fh) – 1000BASE-T Status Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	0	
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	0	
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	1	
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	1	
11:0	Reserved	RO		0000 00000000	

15.15 – 1000BASE-X FDX Capability

The VSC8221 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.14 – 1000BASE-X HDX Capability

The VSC8221 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.13 – 1000BASE-T FDX Capability

The VSC8221 is 1000BASE-T FDX capable, so this bit is hard-wired to “1”.

15.12 – 1000BASE-T HDX Capability

The VSC8221 is 1000BASE-T HDX capable, so this bit is hard-wired to “1”.

15.11:0 – Reserved

23.2.17 Register 16 (10h) – Reserved

Register 16 (10h) – Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

16.15:0 – Reserved

23.2.18 Register 17 (11h) – Reserved

Register 17 (11h) – Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

17.15:0 – Reserved

23.2.19 Register 18 (12h) – Bypass Control Register

Register 18 (12h) – Bypass Control Register

Bit	Name	Access	States	Reset Value	Sticky
15	Reserved	RO		0	
14	Bypass 4B5B Encoder/Decoder	R/W	1 = Bypass 4B5B encoder/decoder 0 = Enable 4B5B encoder/decoder	0	
13	Bypass Scrambler	R/W	1 = Bypass scrambler 0 = Enable scrambler	0	
12	Bypass Descrambler	R/W	1 = Bypass descrambler 0 = Enable descrambler	0	
11:9	Reserved	RO		000	
8	Transmitter Test Clock Enable	R/W	1 = Enable internal TXCLK test output on CLK-OUTMICRO pin 0 = Disable internal TXCLK test output on CLK-OUTMICRO pin	0	

Register 18 (12h) – Bypass Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
7:6	Reserved	RO		01	
5	Disable Automatic Pair Swap Correction	R/W	1=Disable 0=Enable	0	
4	Disable Polarity Inversion	R/W	1=Disable 0=Enable	0	
3	Parallel-Detect Control	R/W	1 = Do not ignore advertised ability 0 = Ignore advertised ability	1	S
2	Reserved	RO		0	
1	Disable Automatic 1000BASE-T Next-Page Exchange	R/W	1 = Disable automatic 1000BASE-T Next-Page exchanges 0 = Enable automatic 1000BASE-T Next-Page exchanges	0	S
0	CLKOUT Output Enable	R/W	1 = Enable output clock pins CLKOUT 0 = Disable output clock pins CLKOUT	1	S

18.15 – Reserved

18.14 – Bypass 4B5B Encoder/Decoder [1]

When bit 18.14 is set to “1”, the 5B codes (TXER and TXD[3:0]) will be passed from the MII interface directly to the scrambler, bypassing the 4B5B encoder. Note that in this mode, J/K and T/R code insertion will not be performed. The receiver will pass descrambled/aligned 5B codes directly to the MII interface (RXER and RXD[3:0]), bypassing the 4B5B decoder. Carrier sense (CRS) is still asserted when a valid frame is detected.

18.13 – Bypass Scrambler[2]

When bit 18.13 is set to “1”, the scrambler is disabled.

18.12 – Bypass Descrambler[2]

When bit 18.12 is set to “1”, the descrambler is disabled.

18.11:9 – Reserved

18.8 – Transmitter Test Clock Enable

When a “1” is written to bit 18.8, the CLKOUTMICRO output pin becomes a test pin for the transmit clock “TXCLK”. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2002, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2002, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TXCLK, is measured. The corresponding edge of TXCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

While transmitter test mode clock TXCLK is intended only for characterization test purposes, CLKOUTMICRO is intended to serve as a general purpose system or MAC reference clock.

18.7:6 – Reserved

[1]This bit applies only in 100BASE-TX mode.

[2]This bit applies only in 100BASE-TX and 1000BASE-T modes.

18.5 - Disable Automatic Pair Swap Correction

When set to ‘1’, the automatic pair swap correction feature of the PHY is disabled.

18.4 - Disable Polarity Inversion

When set to ‘1’, the automatic polarity inversion feature of the PHY is disabled.

18.3 – Parallel-Detect Control

When bit 18.3 is “1”, MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting 18.3 to a “0” will result in auto-negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY.

18.2 – Reserved

18.1 – Disable Automatic 1000BASE-T Next-Page Exchanges

Bit 18.1 is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3-2002 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. You then have the complete responsibility to both of the following:

- Send the correct sequence of Next-Pages to the Link Partner.
- Determine common capabilities and force the device into the correct configuration following successful exchange of pages.

When bit 18.1 is reset to “0”, the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the auto-negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange.

If both bit 18.1 and MII Register bit 4.15 are reset when an auto-negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either auto-negotiation completes or fails. See the description of MII Register bit 4.15 for more details on standard Next-Page exchanges.

18.0 – CLKOUT Output Enable

When bit 18.0 is set to “1”, the VSC8221 provides a 125MHz clock on the CLKOUT output pin. The electrical specification for this clock corresponds to the current settings for VDDIO. This clock is for use by the MAC, system manager CPU, or control logic. By default, this pin is enabled, which enables the clock output independent of the status of any link, unless the hardware reset is active (which also powers down the PLL). When disabled, the clock pins are normally driven low.

23.2.20 Register 19 (13h) – Reserved

Register 19 (13h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

19.15:0 - Reserved

23.2.21 Register 20 (14h) – Reserved

Register 20 (14h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

20.15:0 – Reserved

23.2.22 Register 21 (15h) – Reserved

Register 21 (15h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

21.15:0 – Reserved

23.2.23 Register 22 (16h) – Control & Status Register

Register 22 (16h) – Control & Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Disable Link Integrity State Machine	R/W	1 = Disable link integrity test 0 = Enable link integrity test	0	S
14	Disable jabber Detect	R/W	1 = Disable jabber detect 0 = Enable jabber detect	0	S
13	Reserved	RO		0	
12	SQE Disable Mode	R/W	1=Disable SQE Transmit 0=Enable SQQ Transmit	CMODE	S
11:10	10BASE-T Squelch Control	R/W	00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Reserved	00	S
9	Sticky Reset Enable	R/W	1 = All bits marked as sticky will retain their values during software reset 0 = All bits marked as sticky will be changed to default values during software reset	1	SS
8	EOF Error	RO SC	1 = EOF error detected since last read 0 = EOF error not detected since last read	0	
7	10BASE-T Disconnect State	RO SC	1 = 10BASE-T link disconnected 0 = 10BASE-T link connected	0	
6	10BASE-T Link Status	RO	1 = 10BASE-T link active 0 = 10BASE-T link inactive	0	
5:0	Reserved	RO		000000	

22.15 – Disable Link-Integrity State Machine[1]

When bit 22.15 is set to “0”, the VSC8221 link integrity state machine runs automatically. When bit 22.15 is set to “1”, the link integrity state machine is bypassed and the PHY is forced into link pass status.

22.14 – Disable Jabber Detect[1]

When bit 22.14 is set to “0”, the VSC8221 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When bit 22.14 is set to “1”, transmission requests are allowed to be arbitrarily long without shutting down the transmitter.

22.13 – Reserved

22.12 – SQE Disable Mode[2]

When bit 22.12 is set to “1”, SQE (Signal Quality Error) pulses are not sent. Note that this control bit applies in 10BASE-T HDX mode only.

22.11:10 – 10BASE-T Squelch Control[2]

When bits 22.11:10 are set to “00”, the VSC8221 uses the squelch threshold levels prescribed by the IEEE’s 10BASE-T specification. When bits 22.11:10 are set to “01”, the squelch level is decreased, which may improve the bit error rate performance on long loops. When bits 22.11:10 are set to “10”, the squelch level is increased, which may improve the bit error rate in high-noise environments.

22.9 - Sticky Reset Enable

When bit 22.9 is set, all MII register bits that are marked with an “S” in the “sticky” column will retain their values during a software reset. When cleared, all MII register bits that are marked with an “S” in the “sticky” column will be changed to their default values during a software reset. Note that bits marked with an “SS” retain their values across software reset regardless of the setting of bit 22.9.

22.8 – EOF Error[2]

When bit 22.8 returns a “1”, a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to “0” when it is read.

22.7 – 10BASE-T Disconnect State

Bit 22.7 is set to “1” if the 10BASE-T connection has been broken by the carrier integrity monitor since the last read of this bit. Otherwise, this bit is set to “0”.

22.6 – 10BASE-T Link Status

Bit 22.6 is set to “1” if the 10BASE-T link is active. Otherwise, this bit is set to “0”.

22.5:0 – Reserved

[1]This bit applies only in 10BASE-T mode.
[2]This bit applies only in 10BASE-T HDX mode.

23.2.24 Register 23 (17h) – PHY Control Register #1

Register 23 (17h) – PHY Control Register #1					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:12	MAC/Media Interface Mode Select	RWSW	See Table 33 below	CMODE	
11:4	Reserved[1]	RO		1010 0010	
3	Far End (Media-Side) Loopback Enable	R/W	1 = Far End (Media side) loopback is enabled 0 = Far End (Media side) loopback is disabled	0	
2:1	MAC/Media Interface Mode Select	RWSW	See Table 33 below	CMODE	
0	EEPROM Status	RO	1 = EEPROM is detected on EEPROM interface 0 = EEPROM is not detected on EEPROM interface	0	

[1] Writes to MII Register 23 must preserve the value of bits 11:4, i.e., all writes to MII Register 23 must be in the format xA2xh.

23.15:12, 2:1– MAC/Media Interface Mode Select

Bits 23.15:12 and 23.2:1 are used to select the MAC interface modes and media interface modes. The reset value for these bits is dependent upon the state of the MAC Interface bits in the CMODE hardware configuration. All combinations of these bits not indicated below are reserved:

Table 33. PHY Operating Modes

Operating Mode Category	MII Register 23.15:12, 23.2:1	CMODE2 [3:0]	MAC Interface	Media Interface	Other Settings
Serial MAC PHY Operating Modes	1111,00	0100	802.3z SerDes	CAT5	Clause 37 disabled
	1110, 01	1110	802.3z SerDes	CAT5	Clause 37 enabled
	1110,10	1010	802.3z SerDes	CAT5	Clause 37 enabled, Media Convertor Mode
	1110,00	0000	802.3z SerDes	CAT5	With Clause 37 Auto-Negotiation Detection
	1010,01	1111	SGMII	CAT5	625Mhz SCLK Clock Disabled
	1000,01	0101	SGMII	CAT5	625MHz SCLK Clock Enabled
	1001,00		SGMII	CAT5	Modified Clause 37 Auto-Negotiation disabled, 625MHz SCLK Clock Enabled
	1011,00		SGMII	CAT5	Modified Clause 37 Auto-Negotiation disabled, 625MHz SCLK Clock Disabled

Note: For more information about VSC8221 operating modes, see *Designing a Copper SFP using the VSC8221* application note available on the Vitesse Web site.

23.11:4 – Reserved

Writes to MII Register 23 must preserve the value of bits 11:4, i.e., all writes to MII Register 23 must be in the format xA2xh.

23.3 – Far End (Media-Side) Loopback Enable

When bit 23.3 is set to “1”, all incoming data from the link partner on the media interface is retransmitted back to the link partner on the media interface. In addition, the incoming data will also appear on the RDP/RDN pins of the MAC interface. Any data present on the TDP/TDN pins of the MAC interface is ignored by the VSC8221 when bit 23.3 is set. In order to avoid loss of data, bit 23.3 should not be set while the VSC8221 is receiving data on the media interface. Bit 23.3 applies to all operating modes of the VSC8221. When bit 23.3 is cleared, the VSC8221 resumes normal operation. This bit is cleared by default. Refer to Section 17.3 on page 51.

23.0 – EEPROM Status

When bit 23.0 is set to “1”, an EEPROM has been detected on the external EEPROM interface. When cleared, bit 23.0 indicates that no EEPROM has been detected.

23.2.25 Register 24 (18h) – PHY Control Register #2

Register 24 (18h) – PHY Control Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:13	Reserved[1]	RO		111	S
12	Enable PICMG Miser Mode[2]	R/W	1 = PICMG miser mode is enabled 0 = PICMG miser mode is disabled	0	S
11:10	Reserved	RO		00	
9:7	TX FIFO Depth Control	R/W	000 to 010 = Reserved 011 = Jumbo packet mode 100 = IEEE mode 101 to 111 = Reserved	100	S
6:4	RX FIFO Depth Control	R/W	000 to 010 = Reserved 011 = Jumbo packet mode 100 = IEEE mode 101 to 111 = Reserved	100	S
3:1	Reserved	RO		000	
0	Connector Loopback	R/W	1 = Active (See Section 17.3 on page 51 for details) 0 = Disable	0	

[1] These bits must always be written to as ‘111’.
[2] See Section 11 on page 32 for more information.

24.15:13 – Reserved

These bits must always be written to as ‘111’.

24.12 - Enable PICMG Miser Mode[1]

Setting bit 24.12 turns off some portions of the PHY's DSP block and reduces the PHY's Operating power. This bit can be set in order to reduce power consumption in applications where the signal to noise ratio on the CAT-5 media is high, such as ethernet over the backplane or where the cable length is short (<10m).

[1]See Section 11 on page 32 for more information.

24.11:10 - Reserved

24.9:7 – TX FIFO Depth Control[1]

Bits 24.9:7 control symbol buffering for the transmit synchronization FIFO used in all 1000BT modes. An internal FIFO is used to synchronize the clock domains between the MAC transmit clock and the PHY's clock (e.g., REFCLK), used to transmit symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

24.6:4 – RX FIFO Depth Control[1]

Used in 1000BT , bits 24.6:4 control symbol buffering as determined by the receive synchronization FIFO. An internal FIFO is used to synchronize the clock domains between the MAC receive clock and the PHY's clock (e.g., REFCLK), used to receive symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

24.3:1 – Reserved

24.0 - Connector Loopback

See Section 17.3 on page 51 for details.

23.2.26 Register 25 (19h) – Interrupt Mask Register

Register 25 (19h) – Interrupt Mask Register

Bit	Name	Access	States	Reset Value	Sticky
15	Interrupt Pin Enable	R/W	1 = Enable interrupt pin 0 = Disable interrupt pin	0	S
14	Reserved	RO		0	
13	Link State-Change Interrupt Mask	R/W	1 = Enable Link State/ Energy Detect interrupt 0 = Disable Link State/ Energy Detect interrupt	0	S
12	Reserved	RO		0	
11	Auto-Negotiation Error Interrupt Mask	R/W	1 = Enable Auto-Negotiation Error interrupt 0 = Disable Auto-Negotiation Error interrupt	0	S
10	Auto-Negotiation-Done / Interlock Done Interrupt Mask	R/W	1 = Enable Auto-Negotiation-Done/ Interlock Done interrupt 0 = Disable Auto-Negotiation-Done/ Interlock Done interrupt	0	S
9	Inline Powered Device Detected Interrupt Mask	R/W	1 = Enable Inline Powered Device Detected interrupt 0 = Disable Inline Powered Device Detected interrupt	0	S
8	Symbol Error Interrupt Mask	R/W	1 = Enable Symbol Error interrupt 0 = Disable Symbol Error interrupt	0	S
7	Descrambler Lock-Lost Interrupt Mask	R/W	1 = Enable Lock-Lost interrupt 0 = Disable Lock-Lost interrupt	0	S

[1]The TX and RX FIFOs are not used for 10BASE-T and 100BASE-TX.

Register 25 (19h) – Interrupt Mask Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
6	TX FIFO Interrupt Mask	R/W	1 = Enable TX FIFO interrupt 0 = Disable TX FIFO interrupt	0	S
5	RX FIFO Interrupt Mask	R/W	1 = Enable RX FIFO interrupt 0 = Disable RX FIFO interrupt	0	S
4	Reserved	RO		0	
3	False Carrier Interrupt Mask	R/W	1 = Enable False Carrier interrupt 0 = Disable False Carrier interrupt	0	S
2	Cable Impairment Detect Interrupt Mask	R/W	1 = Enable Cable Impairment Detect interrupt 0 = Disable Cable Impairment Detect interrupt	0	S
1	MASTER/SLAVE Resolution Error Interrupt Mask	R/W	1 = Enable MASTER/SLAVE interrupt 0 = Disable MASTER/SLAVE interrupt	0	S
0	RXER Interrupt Enable	R/W	1 = Enable RX_ER interrupt 0 = Disable RX_ER interrupt	0	S

25.15 – Interrupt Pin Enable

When bit 25.15 is set to “1”, the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT) can be influenced by the state of the Interrupt Status bit (26.15). When bit 25.15 is set to “0”, the interrupt status bits (Register 26) continue to be set in response to interrupts, but the interrupt hardware pin MDINT on the VSC8221 will not be influenced by this particular PHY.

25.14 – Reserved

25.13 – Link State-Change Interrupt Mask

When bit 25.13 is set to “1”, the Link State-Change / Energy Detect interrupt is enabled.

25.12 – Reserved

25.11 – Auto-Negotiation Error Interrupt Mask

When bit 25.11 is set to “1”, the Auto-Negotiation Error Interrupt is enabled.

25.10 – Auto-Negotiation-Done / Interlock Done Interrupt Mask

When bit 25.10 is set to “1”, the Auto-Negotiation-Done Interrupt is enabled.

25.9 – Inline Powered Device Detected Interrupt Mask

When bit 25.9 is set to “1”, the Inline Powered Device Detected Interrupt is enabled.

25.8 – Symbol Error Interrupt Mask

When bit 25.8 is set to “1”, the Symbol Error Interrupt is enabled.

25.7 – Descrambler Lock-Lost Interrupt Mask

When bit 25.7 is set to “1”, the Descrambler Lock-Lost Interrupt is enabled.

25.6 – TX FIFO Interrupt Mask

When bit 25.6 is set to “1”, the TX FIFO Interrupt is enabled.

25.5 – RX FIFO Interrupt Mask

When bit 25.5 is set to “1”, the RX FIFO Interrupt is enabled.

25.4 – Reserved

25.3 – False Carrier Interrupt Mask

When bit 25.3 is set to “1”, the False Carrier Interrupt is enabled.

25.2 – Cable Impairment Detect Interrupt Mask[1]

When bit 25.2 is set to “1”, the Cable Impairment Detect Interrupt is enabled.

25.1 – MASTER/SLAVE Resolution Error Interrupt Mask

When bit 25.1 is set to “1”, the MASTER/SLAVE Resolution Error Interrupt is enabled.

25.0 – RXER Interrupt Enable

When bit 25.0 is set to “1”, the RXER Interrupt is enabled.

23.2.27 Register 26 (1Ah) – Interrupt Status Register

Register 26 (1Ah) – Interrupt Status Register

Bit	Name	Access	States	Reset Value	Sticky
15	Interrupt Status	RO SC	1 = Interrupt pending 0 = No interrupt pending	0	
14	Reserved	RO		0	
13	Link State-Change Interrupt Status	RO SC	1 = Link State-Change/ Energy Detect interrupt pending	0	
12	Reserved	RO		0	
11	Auto-Negotiation Error Interrupt Status	RO SC	1 = Auto-Negotiation Error interrupt pending	0	
10	Auto-Negotiation-Done / Interlock Done Interrupt Status	RO SC	1 = Auto-Negotiation-Done/ Interlock Done interrupt pending	0	
9	Inline Powered Device Detected Interrupt Status	RO SC	1 = Inline Powered Device Detected interrupt pending	0	
8	Symbol Error Interrupt Status	RO SC	1 = Symbol Error interrupt pending	0	
7	Descrambler Lock-Lost Interrupt Status	RO SC	1 = Lock-Lost interrupt pending	0	
6	TX FIFO Interrupt Status	RO SC	1 = TX FIFO interrupt pending	0	
5	RX FIFO Interrupt Status	RO SC	1 = RX FIFO interrupt pending	0	
4	Reserved	RO		0	
3	False Carrier Interrupt Status	RO SC	1 = False Carrier interrupt pending	0	
2	Cable Impairment Detect Interrupt Status	RO SC	1 = Cable Impairment Detect interrupt pending	0	
1	MASTER/SLAVE Resolution Interrupt Status	RO SC	1 = MASTER/SLAVE Error interrupt pending	0	
0	RXER Interrupt Status	RO	1 = RXER interrupt pending 0 = No RXER interrupt pending	0	

[1]This interrupt is vaild only when 10/100 speeds are advertised.

26.15 – Interrupt Status

When bit 26.15 is set to “1”, an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read.

26.14 – Reserved

26.13 – Link State-Change Interrupt Status

When the link status of the PHY changes, bit 26.13 is set to “1” if bit 25.13 is also set to “1”. This bit is automatically cleared when read.

26.12 – Reserved

26.11 – Auto-Negotiation Error Interrupt Status

When an error is detected by the Auto-Negotiation state machine, bit 26.11 is set to “1” if bit 25.11 is also set to “1”. This bit is automatically cleared when read.

26.10 – Auto-Negotiation-Done / Interlock Done Interrupt Status

When the auto-negotiation state machine finishes a negotiation process, bit 26.10 is set to “1” if bit 25.10 is also set to “1”. This bit is automatically cleared when read.

26.9 – Inline Powered Device Detected Interrupt Status

When a device requiring inline power over CAT-5 is detected, bit 26.9 is set to “1” if bit 25.9 is also set to “1”. This bit is automatically cleared when read.

26.8 – Symbol Error Interrupt Status

When a symbol error is detected by the descrambler, bit 26.8 is set to “1” if bit 25.8 is also set to “1”. This bit is automatically cleared when read.

26.7 – Descrambler Lock-Lost Interrupt Status

When the descrambler loses lock, bit 26.7 is set to “1” if bit 25.7 is also set to “1”. This bit is automatically cleared when read.

26.6 – TX FIFO Interrupt Status

When the TX FIFO enters an underflow or overflow condition, bit 26.6 is set to “1” if bit 25.6 is also set to “1”. This bit is automatically cleared when read.

26.5 – RX FIFO Interrupt Status

When the RX FIFO enters an underflow or overflow condition, bit 26.5 is set to “1” if bit 25.5 is also set to “1”. This bit is automatically cleared when read.

26.4 – Reserved

26.3 – False Carrier Interrupt Status

When the PHY has detected a false carrier, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read,

26.2 – Cable Impairment Detect Interrupt Status

When the PHY has detected an impairment on the CAT-5 media, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read.

26.1 – MASTER/SLAVE Resolution Error Interrupt Status

When a MASTER/SLAVE resolution error is detected, bit 26.1 is set to “1” if bit 25.1 is also set to “1”. This bit is automatically cleared when read.

26.0 – RXER Interrupt Status

When an RXER condition occurs, bit 26.0 is set to “1” if bit 25.0 is also set to “1”.This bit is automatically cleared when read.

23.2.28 Register 27 (1Bh) – LED Control Register

Register 27 (1Bh) – LED Control Register

Bit	Name	Access	States	Reset Value	Sticky
15:12	Reserved	RO		CMODE	
11:10	LED Pin 2 Configuration	R/W	00 = Link10/Activity 01[1] = Duplex/Collision 10 = Link/Activity 11[2] = Tx	CMODE	S
9:8	LED Pin 1 Configuration	R/W	00 = Link100/Activity 01 = Link10/100/Activity 10 = Link/Activity 11 = Link100/1000/Activity	CMODE	S
7:6	LED Pin 0 Configuration	R/W	00 = Link1000/Activity 01 = Link/Activity w/ Serial output on LED pins 1 and 2 10 = Fault 11 = Rx	CMODE	S
5	LED Pulse-stretch Rate/ Blink Rate	R/W	0 = 5 Hz blink rate/200 ms pulse-stretch 1 = 10 Hz blink rate/100 ms pulse-stretch	0	S
4	LED Pulsing Enable	R/W	1 = Enable 5 kHz, 20% duty cycle LED pulsing for power savings 0 = LED pulsing disabled	0	S
3	LED Pulse-Stretch / Blink Select	R/W	1 = Collision, Activity, Rx and Tx functions will flash at a rate selected by Blink/Pulse-Stretch Rate bits 0 = Collision, Activity, Rx and Tx functions will blink at a rate selected by Blink/Pulse-Stretch Rate bits	0	S
2	Link/Activity Behaviour	R/W	1 = Link function indicates link status only 0 = Link/Activity function will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.	0	
1	LED Linkxxxx/Activity[3] Behavior	R/W	1 = Link function indicates link status only 0 = All link functions will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.	0	S
0	LED Duplex/Collision Behavior	R/W	1 = Duplex function indicates duplex status only 0 = Duplex function will blink or flash when collision is present	0	S

[1] This setting is ‘Force off’ when MII Register 20E.13 is set.
[2] This setting is ‘Force on’ when MII Register 20E.13 is set.
[3] Linkxxxx/Activity stands for Link10/Activity,Link100/Activity,Link1000/Activity,Link10/100/Activity and Link100/1000/Activity. Its definition does not include the Link/Activity function.

27.15:12 - Reserved

27.11:6 – LED Pin Configuration

Each of the three LED pins on the VSC8221 can be configured for one of four functions. These functions are different for each LED pin.[1] Bits 27.11:6 are used to select the function for each LED pin. The reset value of these bits is set by the LED configuration bits in the CMODE hardware configuration.

7.5 – LED Pulse-Stretch/Blink Rate

The Collision, Activity, Tx and Rx LED functions can be set to either blink at a constant rate or visibly flash through the use of pulse-stretching. The blink rate and pulse-stretch length are set with this bit.

27.4 – LED Pulsing Enable

When bit 27.4 is set to “1”, all LED outputs are pulsed at a 5kHz rate with 20% duty cycle in order to save power.

27.3 – LED Pulse-Stretch / Blink Select

When bit 27.3 is set to “1”, Collision, Activity, Tx and Rx LED functions will be pulse-stretched. When bit 27.3 is cleared, these LED functions will blink at a constant rate. Bit 27.5 are used to select the pulse-stretch / blink rate.

27.2 – LED Link/Activity Behavior

When bit 27.2 is set to “0”, the link status LED function will blink or flash when activity is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

27.1 – LED Linkxxxx/Activity Behavior

When bit 27.1 is set to “0”, all linkxxxx status LED functions (Link10, Link100, Link1000, Link10/100, Link100/1000) will blink or flash when activity is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

27.0 – LED Duplex/Collision Behavior

When bit 27.0 is set to “1”, the Duplex LED function indicates duplex status only. When bit 27.0 is cleared, the Duplex function will blink or flash when collision is present. Blink / flash behavior is selected by bits 27.3 and 27.5.

[1]Note that if bits 27.7:6 are set to “01”, LED pins 1 and 2 are used as serial output pins and the values of bits 27.11:8 are ignored.

23.2.29 Register 28 (1Ch) – Auxiliary Control and Status Register

Register 28 (1Ch) – Auxiliary Control and Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Auto-Negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation not complete	0	
14	Auto-Negotiation Disabled	RO	1 = Auto-negotiation was disabled 0 = Auto-negotiation is enabled	0	
13	MDI/MDI-X Crossover Indication	RO	1 = MDI/MDI-X crossover detected 0 = MDI/MDI-X crossover not detected	0	
12	CD Pair Swap	RO	1 = CD pairs are swapped 0 = CD pairs are not swapped	0	
11	A Polarity Inversion	RO	1 = Polarity swapped on pair A 0 = Polarity not swapped on pair A	0	
10	B Polarity Inversion	RO	1 = Polarity swapped on pair B 0 = Polarity not swapped on pair B	0	
9	C Polarity Inversion	RO	1 = Polarity swapped on pair C 0 = Polarity not swapped on pair C	0	
8	D Polarity Inversion	RO	1 = Polarity swapped on pair D 0 = Polarity not swapped on pair D	0	
7	Reserved	RO	-	--	
6	Enhanced ActiPHY Mode Enable	R/W	1 = Enable enhanced ActiPHY power management 0 = Disable enhanced ActiPHY power management	0	S
5	FDX Status	RO	1 = Full Duplex 0 = Half Duplex	0	
4:3	Speed Status	RO	00 = Speed is 10BASE-T 01 = Speed is 100BASE-TX or 100BASE-FX 10 = Speed is 1000BASE-T 11 = Reserved	00	
2	Reserved[1]	RO		1	
1:0	Enhanced ActiPHY™ Sleep Timer	R/W	00=1 second 01=2 seconds 10-3 seconds 11=4 seconds	01	

[1] This bit must always be set to '1'.

28.15 – Auto-Negotiation Complete

This bit is a copy of bit 1.5, duplicated here for convenience.

28.14 – Auto-Negotiation Disabled

When bit 28.14 is read as a "1", this bit indicates that the auto-negotiation process has been disabled. This happens only when register bit 0.12 is set to "0".

28.13 – MDI/MDI-X Crossover Indication

When bit 28.13 returns a "1", the auto-negotiation state machine has determined that crossover does not exist in the signal path. The crossover will therefore be performed internally to the PHY, as described by the MDI/MDI-X crossover specification.[1]

[1]This bit is valid only after descrambler lock has been achieved and as long as bit 18.5 is set to "0".

28.12 – CD Pair Swap[1]

When bit 28.12 returns a “1”, the PHY has determined that subchannel cable pairs C and D have been swapped between the far-end transmitted and the receiver. When bit 28.12 returns a “1”, the PHY internally swaps pairs C and D (as long as bit 18.5 is set to “0”).[1]

28.11 – A Polarity Inversion

When bit 28.11 returns a “1”, the PHY has determined that the polarity of subchannel cable pair A has been inverted between the far-end transmitter and the near-end receiver. When bit 28.11 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.11 is valid only when bit 1.5 is set to “1”.

28.10 – B Polarity Inversion

When bit 28.10 returns a “1”, the PHY has determined that the polarity of subchannel cable pair B has been inverted between the far-end transmitter and the near-end receiver. When bit 28.10 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.10 is valid only when bit 1.5 is set to “1”.

28.9 – C Polarity Inversion[2]

When bit 28.9 returns a “1”, the PHY has determined that the polarity of subchannel cable pair C has been inverted between the far-end transmitter and the near-end receiver. When bit 28.9 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.9 is valid only when bit 1.5 is set to “1”.

28.8 – D Polarity Inversion[1]

When bit 28.8 returns a “1”, the PHY has determined that the polarity of subchannel cable pair D has been inverted between the far-end transmitter and the near-end receiver. When bit 28.8 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.8 is valid only when bit 1.5 is set to “1”.

28.7 – Reserved

28.6 - Enable Enhanced ActiPHY Mode

When bit 28.6 is set to a “1”, the enhanced ActiPHY power management mode is set in the VSC8221. The reset value for this bit is determined by the Enhanced ActiPHY bit in the CMODE hardware configuration.

28.5 – FDX Status

Bit 28.5 indicates the actual FDX/HDX operating mode of the PHY.

28.4:3 – Speed Status

Bits 27.4:3 indicate the actual operating speed of the PHY.

28.2 – Reserved

This bit must always be set to ‘1’.

28.1:0 - Enhanced ActiPHY™ Sleep Timer

This sets the time period the PHY stays in ‘Low Power’ State when Enhanced ActiPHY™ mode is enabled, before entering the ‘LP Wake-up State’. Refer to Section 15 on page 47 for details.

[1]This bit applies only in 1000BASE-T mode.
[2]This bit applies only in 1000BASE-T mode.

23.2.30 Register 29 (1Dh) – Reserved

Register 29 (1Dh) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

29.15:0 - Reserved

23.2.31 Register 30 (1Eh) - MAC Interface Clause 37 Auto-Negotiation Control and Status

Register 30 (1Eh) – MAC Interface Clause 37 Auto-Negotiation Control and Status					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Reserved	RO		0	
14	Clause 37 Auto-Negotiation Disable	R/W	1 = Disable clause 37 auto-negotiation 0 = Enable clause 37 auto-negotiation	0	S
13:12	MAC Remote Fault	RO	Correspond to remote fault bits sent by MAC during clause 37 auto-negotiation	00	
11	MAC Asymmetric Pause	RO	Corresponds to Asymmetric Pause bit sent by MAC during clause 37 auto-negotiation	0	
10	MAC Symmetric Pause	RO	Corresponds to Symmetric Pause bit sent by MAC during clause 37 auto-negotiation	0	
9	Clause 37 Restart Auto-Negotiaton	R/W SC	1 = Initiate restart of clause 37 auto-negotiation 0 = Normal operation	0	
8	MAC Full Duplex	RO	Corresponds to Full Duplex Ability bit sent by MAC during clause 37 auto-negotiation	0	
7	MAC Half Duplex	RO	Corresponds to Half Duplex Ability bit sent by MAC during clause 37 auto-negotiation	0	
6	Reserved	RO		0	
5	Clause 37 Auto-Negotiation Complete	RO	1 = Clause 37 auto-negotiation has completed successfully 0 = Clause 37 auto-negotiation has not completed	0	
4	Reserved	RO		0	
3	Link Interlock Fail	RO	1 = Clause 37/28 auto-negotiation interlock could not complete	0	
2	Link Interlock Complete	RO	1 = Clause 37/28 auto-negotiation interlock completed	0	
1:0	RXLOS Pulse Delay[1]	R/W	00 = 0ms (always stays low) 01 = 20ms 10 = 200ms 11 = 500ms	01	

[1] In SGMII to CAT-5, Modified Clause 37 Auto-negotiation-Enabled PHY Operating modes, the RXLOS signal is always driven, regardless of the settings of MII Register 30.1:0. For more information about PHY operating modes, see Table 33, “PHY Operating Modes,” on page 86.

30.15 – Reserved

30.14 - Clause 37 Auto-Negotiation Disable

When bit 30.14 is set to a “1”, the clause 37 auto-negotiation state machine is disabled in the VSC8221. Bit 30.14 is cleared by default.

30.13:12 - MAC Remote Fault

Bits 30.13:12 correspond to the Remote Fault bits sent to the VSC8221 by the MAC during the clause 37 auto-negotiation process.

30.11 - MAC Asymmetric Pause

Bit 30.11 corresponds to the Asymmetric Pause bit sent to the VSC8221 by the MAC during the clause 37 auto-negotiation process.

30.10 - MAC Symmetric Pause

Bit 30.10 corresponds to the Symmetric Pause bit sent to the VSC8221 by the MAC during the clause 37 auto-negotiation process.

30.9 - Clause 37 Restart Auto-Negotiation

When bit 30.9 is set to a “1”, the clause 37 auto-negotiation process is restarted. This bit is self-clearing and always reads back as “0”.

30.8 - MAC Full Duplex

Bit 30.8 corresponds to the Full Duplex Ability bit sent to the VSC8221 by the MAC during the clause 37 auto-negotiation process.

30.7 - MAC Half Duplex

Bit 30.7 corresponds to the Half Duplex Ability bit sent to the VSC8221 by the MAC during the clause 37 auto-negotiation process.

30.6 - Reserved

30.5 - Clause 37 Auto-Negotiation Complete

When bit 30.5 is set to a “1”, the clause 37 auto-negotiation has completed successfully.

30.4 - Reserved

30.3 - Link Interlock Fail

Bit 30.3 is set to indicate a failure to complete interlock between Clause-37 auto-negotiation and Clause-28 auto-negotiation. This bit is valid only in SerDes to CAT5 PHY operating modes.

30.2 - Link Interlock Complete

Bit 30.2 is set to indicate a complete interlock between Clause-37 auto-negotiation and Clause-28 auto-negotiation. This bit is valid only in SerDes to CAT5 PHY operating modes.

30.1:0 - RXLOS Pulse Delay

Bits 30.1:0 specify the RXLOS Pulse Delay. It sets the time the RXLOS/SIGDET signal pin is asserted when the CAT5 Media Link is dropped. This bit is only valid when the ‘SFP Mode’ bit Extended MII Register 21E.15 = “1”.

23.2.32 Register 31 (1Fh) – Extended Page Access

Register 31 (1Fh) – Extended Page Access[1]

Bit	Name	Access	States	Reset Value	Sticky
15:1	Reserved	RO		00000000 0000000	
0	Extended Page Access	R/W	1 = MII registers 16:30 will access extended register set 0 = MII registers 16:30 will access standard register set	0	

[1] This register will always read zero.

31.15:1 – Reserved

31.0 - Extended Page Access

In order to provide additional functionality beyond the IEEE802.3 specified 32 MII registers, the VSC8221 contains an extended register set which supports an additional 15 registers. When bit 31.0 is set to a “1”, MII registers 16:30 will access the extended set of registers. The state of bit 31.0 has no effect on MII registers 0:15.

23.3 Extended MII Registers

23.3.1 Register 16E (10h) - Reserved

Register 16E (10h) – Reserved

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

16E.15:0 – Reserved

23.3.2 Register 17E (11h) - Serdes Control Register

Register 17E (11h) – SerDes Control Register

Bit	Name	Access	States	Reset Value	Sticky
15:5	Reserved	RO		00000000 000	
4:2	RDP/RDN SCLKP/SCLKN Output Swing Control	R/W	000=0.4mv(p-p) 001=0.6mv(p-p) 010=0.8mv(p-p) 011=1.0mv(p-p) 100=1.2mv(p-p) 101=1.4mv(p-p) 110/111=1.6mv(p-p)	100	
1	25mv Hysteresis Disable	R/W	1=Disable 0=Enable	0	
0	CLKOUTMICRO Enable	R/W	1=Enable 0=Disable	1	

17E.15:5 - Reserved

17E.4:2 - RDP/RDN SCLKP/SCLKN Output Swing Control

These bits set the output swing amplitude (peak-to-peak voltage) on the RDP/RDN SCLKP/SCKLN Output Swing output pins.

17E.1 - 25mv Hysteresis Disable

When set, this bit disables the 25mv Hysteresis built into the TDP/TDN and SDIP/SDIN high speed differential input pins.

17E.0 - CLKOUTMICRO Enable

When set, the CLKOUTMICRO clock output is enabled.

23.3.3 Register 18E (12h) - Reserved

Register 18E (12h) – Reserved

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000001 11111111	

18E.15:0 - Reserved

23.3.4 Register 19E (13h) - SerDes Control # 2

Register 19E (13h) – SerDes Control #2

Bit	Name	Access	States	Reset Value	Sticky
15:2	Reserved	RO		00000000 00000000	
1	SIGDET Pin Direction	R/W	0 = Input 1 = Output	CMODE	
0	SIGDET Pin Polarity	R/W	0 = Active High 1 = Active Low	0	

19E.15:2 - Reserved

19E.1 - SIGDET Pin Direction

This bit is valid in non-SFP modes i.e. when MII Register 21E.15 is clear. In non-SFP mode, the RXLOS/SIGDET pin behaves like the SIGDET pin. When set as an input, the assertion of the SIGDET pin enables the SerDes block in Serial MAC to CAT5 category of PHY operating modes. When set as an output in Serial MAC to CAT5 Media operating modes, the SIGDET pin is asserted when the CAT5 Media link is up. In Fiber Media operating modes, the SIGDET output is asserted if the PHY sees valid 8B/10B encoded signals on the TDP/TDN pins.

19E.0 - SIGDET Pin Polarity

This bits sets the assertion polarity of the SIGDET pins. This bit is valid in both cases i.e when SIGDET is an input or an output.

23.3.5 Register 20E (14h) - Extended PHY Control Register #3

Register 20E (14h) – Extended PHY Control Register #3					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Disable Byte Sync	R/W	0 = Enable 1 = Disable	0	S
14	Reserved	RO		0	
13	Enable Force LED	R/W	1 = Enable LED force 0 = Disable LED force	0	S
12:9	Reserved[1]			1000	
8	CLKOUTMICRO Frequency	R/W	1 = 125MHz clock output on CLKOUTMICRO 0 = 4MHz clock output on CLKOUTMICRO	0	S
7:6	Media Mode Status	RO	00 = No media selected 01 = Copper media selected 10 = Reserved 11 = Reserved	0	
5	Serial MAC Interface Line Imped-ance	RO	1=75 ohm impedance. 0=50 ohm impedance	CMODE	S
4	Enable Link Speed Auto-Downshift	R/W	1 = Enable auto link speed downshift 0 = Disable auto link speed downshift	0	S
3:2	Link Speed Auto-Downshift Control	R/W	00 = Downshift after 2 failed attempts 01 = Downshift after 3 failed attempts 10 = Downshift after 4 failed attempts 11 = Downshift after 5 failed attempts	01	S
1	Link Speed Auto-Downshift Status	RO	0 = No downshift 1 = Downshift is required or has occurred	0	
0	Reserved	RO		0	

[1] Writes to Extended MII Register 20E must preserve the value of bits 12:9, i.e., all writes to Extended MII Register 20E must be in the format xxx1000xxxxxxxxxb.

20E.15 Disable Byte Sync

When enabled, the PHY aligns the 10bit data to the boundary of the COMMA character.

20E.14 - Reserved

These bits must always be set to ‘”0”.

20E.13 - Enable LED force

When this bit is set, the LED configuration setting “01” becomes ‘Force off’ and the LED configuration setting “11” becomes ‘Force on’. Refer to Section 23.2.28: "Register 27 (1Bh) – LED Control Register" for details.

20E.12:9 Reserved

Writes to Extended MII Register 20E must preserve the value of bits 12:9, i.e., all writes to Extended MII Register 20E must be in the format xxx1000xxxxxxxxxb.

20E.8 - CLKOUTMICRO Frequency

The frequency of the CLKOUTMICRO pin can be changed by using bit 20E.8.

20E.7:6 - Media Mode Status

Bits 20E.7:6 reflect the media interface status.

20E.5 - SerDes Line Impedance

The internal termination impedance of the high speed serial interface inside the VSC8221 can be selected using bit 20E.5. This applies to the SerDes/SGMII pins on the device. The reset value of this bit is determined by the SerDes Line Impedance bit in the CMODE hardware configuration.

20E.4 - Enable Link Speed Auto-Downshift

When bit 20E.4 is set to a “1”, the VSC8221 will “downshift” the auto-negotiation advertisement to 100BASE-TX after the number of failed 1000BASE-T auto-negotiation attempts specified in bits 20E.3:2. The reset value of this bit is determined by the Link Speed Downshift bit in the CMODE hardware configuration.

20E.3:2 - Link Speed Auto-Downshift Control

Bits 20E.3:2 determine the number of unsuccessful 1000BASE-T auto-negotiation attempts that are required before the auto-negotiation advertisement is “downshifted” to 100BASE-TX. These bits are valid only if bit 20E.4 is set.

20E.1 - Link Speed Auto-Downshift Status

When bit 20E.1 is set to a “1” and bit 20E.4 is set to a “1”, the current link speed is the result of a “downshift” to 100BASE-TX. When bit 20E.1 is set to a “1” and bit 20E.4 is cleared, the current link requires a “downshift” in order to be established.

20E.0 - Reserved

23.3.6 Register 21E (15h) - EEPROM Interface Status and Control Register

Register 21E (15h) - EEPROM Interface Status and Control Register

Bit	Name	Access	States	Reset Value	Sticky
15	SFP MODE	R/W	1 = SFP MODE 0 = IEEE MODE	CMODE	SS
14	Re-Read EEPROM on Software Reset	R/W	1 = Contents of EEPROM should be re-read on software reset 0 = Contents of EEPROM should not be re-read on software reset	0	SS
13	EEPROM Access Enable	R/W SC	1 = Execute read or write to EEPROM	0	
12	EEPROM Read/Write	R/W	1 = Read from EEPROM 0 = Write to EEPROM	1	
11	EEPROM Ready[1]	RO	1 = EEPROM is ready for read/write 0 = EEPROM is busy	1	
10:0	EEPROM Address	R/W	EEPROM address to read/write	000 00000000	

[1] After an EEPROM write operation, the station manager or controller must wait an additional 10 ms before performing the next EEPROM read or write operation. This delay is needed for the EEPROM to complete its internal memory write process. Note that this additional wait is not needed after an EEPROM read operation.

21E.15 - SFP MODE

SFP Mode (bit 15 =”1”) sets the following PHY defaults:

- TXDIS/$\overline{\text{SRESET}}$ is active high, i.e. behaves like TXDIS.
- MODDEF0/CLKOUT pin functions like MODDEF0, i.e this pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI interface.
- RXLOS/SIGDET pins functions like RXLOS.
- The SMI interface is set in MSA mode.

IEEE Mode (bit 15 = “0”) sets the following PHY defaults:

- TXDIS/$\overline{\text{SRESET}}$ is active low, i.e. behaves like $\overline{\text{SRESET}}$.
- MODDEF0/CLKOUT pin functions like CLKOUT, i.e this pin drives out a 125MHz clock.
- RXLOS/SIGDET pin functions like SIGDET.
- The SMI interface is set in IEEE mode.

21E.14 - Re-Read EEPROM on Software Reset

When bit 21E.14 is set to a “1”, the contents of the EEPROM will be re-read and reloaded into the MII registers upon software reset.

21E.13 - EEPROM Access Enable

When bit 21E.13 is set to a “1”, the EEPROM address in bits 21E.10:0 is written to or read from, based on the state of bit 21E.12. The data to read/write resides in register 22E.

21E.12 - EEPROM Read/Write

When bit 21E.12 is set to a “1”, the VSC8221 will read from the EEPROM when bit 21E.13 is set. When bit 21E.12 is cleared, the VSC8221 will write to the EEPROM when bit 21E.13 is set.

21E.11 - EEPROM Ready

When the VSC8221 is busy reading/writing to the EEPROM, bit 21E.11 will be cleared. Bit 21E.13 should not be set while bit 21E.11 is cleared.

21E.10:1 - EEPROM Address

These bits contain the EEPROM address that the VSC8221 will read from or write to when bit 21E.13 is set.

23.3.7 Register 22E (16h) - EEPROM Data Read/Write Register

Register 22E (16h) - EEPROM Data Read/Write Register

Bit	Name	Access	States	Reset Value	Sticky
15:8	EEPROM Read Data	RO	8-bit data read from EEPROM	00000000	
7:0	EEPROM Write Data	R/W	8-bit data to write to EEPROM	00000000	

22E.15:18 - EEPROM Read Data

After an EEPROM read has occurred by setting bits 21E.13 and 21E.12 to a “1”, the data read from the EEPROM is placed in these bits.

22E.7:0 - EEPROM Write Data

When an EEPROM write is initiated by setting bits 21E.13 to a “1” and clearing bit 21E.12, the data from these bits is written to the EEPROM.

23.3.8 Register 23E (17h) - Extended PHY Control Register #4

Register 23E (17h) - Extended PHY Control Register #4

Bit	Name	Access	States	Reset Value	Sticky
15:11	PHY Address	RO	PHY address latched on reset	CMODE	
10	Enable In-line Powered Device Detection	R/W	1 = In-line powered device detection is enabled 0 = In-line powered device detection is disabled	0	S
9:8	In-line Powered Device Detection Status	RO	00 = Searching for devices 01 = Device found which requires in-line power 10 = Device found which does not require in-line power 11 = Reserved	00	
7:0	CRC Counter	RO SC	CRC counter for Ethernet packet generator	00000000	

23E.15:11 - PHY Address

These bits contain the PHY address of the current PHY port. The reset value of these bits is determined by the PHY Address bits in the CMODE hardware configuration.

23E.10 - Enable In-line Powered Device Detection

When bit 23E.10 is set to a “1”, the VSC8221 will search for devices requiring CAT-5 in-line power as part of the auto-negotiation process.

23E.9:8 - In-line Powered Device Detection Status

Bits 23E.9:8 are used by the station manager to determine if a device which requires in-line power is connected to the VSC8221.

23E.7:0 - CRC Counter

When the Ethernet Packet Generator is enabled by setting MII Register 29.15, these bits count the number of packets received that contain a CRC error. This counter will saturate at FFh and is cleared when read.

23.3.9 Register 24E (18h) - Reserved

Register 24E (18h) - Reserved Register

Bit	Name	Access	States	Reset Value	Sticky
15:0	Reserved	RO		00000000 00000000	

24E.15:0 - Reserved

23.3.10 Register 25E (19h) - Reserved

Register 25E (19h) - Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

25E.15:0 - Reserved

23.3.11 Register 26E (1Ah) - Reserved

Register 26E (1Ah) - Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

26E.15:0 - Reserved

23.3.12 Register 27E (1Bh) - Reserved

Register 27E (1Bh) - Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

27E.15:0 - Reserved

23.3.13 Register 28E (1Ch) - Reserved

Register 28E (1Ch) - Reserved Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		00000000 00000000	

28E.15:0 - Reserved

23.3.14 Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1

Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1[1]					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	EPG Enable	R/W	1 = Enable EPG 0 = Disable EPG	0	
14	EPG Run/Stop	R/W	1 = Run EPG 0 = Stop EPG	0	
13	Transmission Duration	R/W	1 = Continuous 0 = Send 30,000,000 packets and stop	0	
12:11	Packet Length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (jumbo packet)	00	
10	Inter-packet Gap	R/W	1 = 8,192 ns 0 = 96 ns	0	
9:6	Destination Address	R/W	MSB's lower nibble of the 6-byte destination address	0001	
5:2	Source Address	R/W	MSB's lower nibble of the 6-byte source address	0000	
1	TXER Control	R/W	1 = Assert TXER 0 = Do not assert TXER	0	
0	Bad FCS Generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0	

[1] Refer to Section 17.1 on page 51 for more information.

29E.15 - EPG Enable

When bit 29E.15 is set to a "1", the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled. When bit 29E.15 is cleared, the MAC has full control of the PHY transmit signals.

29E.14 - EPG Run/Stop

Bit 29E.14 controls the beginning and end of packet transmission. When this bit is set to a "1", the EPG begins the transmission of packets. When this bit is cleared, the EPG ends the transmission of packets, after the current packet is transmitted. Bit 29E.14 is valid only if bit 29E.15 is set to a "1".

29E.13 - Transmission Duration

When bit 29E.13 is set to a "1", the EPG will continuously transmit packets as long as bit 29E.14 is set to a "1". If bit 29E.13 is cleared, the EPG will begin transmission of 30,000,000 packets when bit 29E.14 is set to a "1", after which time, bit 29E.14 is automatically cleared. If bit 29E.13 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.12:11 - Packet Length

Bits 29E.12:11 select the length of the packets to be generated by the EPG. Note that when these bits are set to "11", a 10,000-byte "jumbo" packet is sent, which may not be compatible with all Ethernet equipment. If bits 29E.12:11 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.10 - Inter-packet Gap

Bit 29E.10 selects the inter-packet gap for packets generated by the EPG. If bit 29E.10 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.9:6 - Destination Address

The 6-byte destination address for packets generated by the EPG is assigned one of 16 values in the range 0xF0 FF FF FF FF FFh through 0xFF FF FF FF FF FFh. The most significant byte's lower nibble bits of the destination address are selected by bits 29E.9:6. If bits 29E.9:6 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.5:2 - Source Address

The 6-byte source address for packets generated by the EPG is assigned one of 16 values in the range 0xF0 FF FF FF FF FFh through 0xFF FF FF FF FF FFh. The most significant byte's lower nibble bits of the source address are selected by bits 29E.5:2. If bits 29E.5:2 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.1 - TXER Control

When bit 29E.1 is set to a "1", all packets generated by the EPG will have the TXER signal asserted. When this bit is cleared, TXER is not asserted. If bit 29E.1 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

29E.0 - Bad FCS Generation

When bit 29E.0 is set to a "1", the EPG will generate packets containing an invalid Frame Check Sequence (FCS). When this bit is cleared, the all EPG packets will contain a valid Frame Check Sequence. If bit 29E.0 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

23.3.15 Register 30E (1Eh) - 1000BASE-T Ethernet Packet Generator Register #2

Register 30E (1Eh) - 1000BASE-T Ethernet Packet Generator Register #2[1]

Bit	Name	Access	States	Reset Value	Sticky
15:0	EPG Packet Payload	R/W	Data for packets generated by EPG	00000000 00000000	

[1] Refer to Section 17.1 on page 51 for more information.

30E.15:0 - EPG Packet Payload

Each packet generated by the EPG contains a repeating sequence of bits 30E.15:0 as the data payload. If bits 30E.15:0 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a "1" again.

24 ELECTRICAL SPECIFICATIONS

24.1 Absolute Maximum Ratings

Stresses listed under the Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 34. Absolute Maximum Ratings

Symbol	Min	Max	Unit	Parameter Description & Conditions
$T_{Storage}$	-65	150	°C	Storage temperature range.
$VDD33A_{(Analog)}$	-0.5	4.0	V	DC voltage on analog I/O supply pin.
VDDREG	-0.5	4.0	V	DC voltage on Regulator supply pin.
VDDIO/VDDI-OMICRO/VDDI-OCTRL	-0.5	4.0	V	DC voltage on any digital I/O supply pin.
$VDD_{(5V)}$	-0.5	5.5	V	DC voltage on any 5 V-tolerant digital input pin.
VDD12	-0.5	1.5	V	DC voltage on any digital core supply pin.
VDD12A	-0.5	1.5	V	DC voltage on any 1.2 V analog supply pin.
$V_{Pin(DC)}$	-0.5	V_{DD} + 0.5	V	DC voltage on any non-supply pin.
$V_{ESD(HBM)}$	2		kV	ESD voltage on any pin, per event, according to the Human Body Model.
CESD	2		kV	Cable-sourced ESD tolerance, per event, at 200 meters.
$I_{LATCHUP}$	-200	+200	mA	T = +85 °C, valid for all I/O signal pins.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

24.2 Recommended Operating Conditions

Table 35. Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
VDD33A	3.0	3.3	3.6	V	DC voltage on VDD33A pins
VDDREG	3.0	3.3	3.6	V	DC voltage on Regulator Supply pin
VDD12A	1.14	1.2	1.26	V	DC voltage on VDD12A pins
VDDIO/ VDDIOMICRO/ VDDIOCTRL	3.0 2.25	3.3 2.5	3.6 2.75	V	DC voltage on VDDIO pins Note: The on-chip I/O calibration is only valid within these recommended operating conditions.

Table 35. Recommended Operating Conditions *(continued)*

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
VDD12	1.14	1.2	1.26	V	DC voltage on VDD12 pins
F_{REFCLK}		25 125		MHz	Local reference clock (REFCLK) nominal frequency. Refer to F_{TOL} for minimum and maximum values.
$F_{TOL\ (REFCLK)}$	-100		+100	ppm	Reference clock frequency offset tolerance over specified temperature range (25 MHz or 125 MHz)
$F_{TOL\ (LINK)}$	-1500		+1500	ppm	CAT5 link partner frequency offset tolerance (for any link speed)
R_{EXT}		2.00		kΩ	External reference circuit bias resistor (1% tolerance).
C_{REF_FILT}		0.1		µF	External reference generator filter capacitor (10% tolerance).
T_{OPER}	0		100	°C	Operating temperature. Lower limit of specification is ambient temperature, and upper limit is case temperature.

24.3 Thermal Application Data

Table 36. Thermal Application Data

Printed Circuit Board Conditions (JEDEC JESD51-9)	
PCB Layers	4
PCB Dimensions (mm x mm)	101.6 × 114.3
PCB Thickness (mm)	1.6
Environment Conditions	
Maximum operating junction temperature (ºC)	125
Ambient free-air operating temperature (ºC)	70
Worst Case Power Dissipation (W)	1

Table 37. Thermal Resistances

Symbol	Typ	Unit	Parameter Description & Conditions
θ_{JA} (0 m/s airflow)	40.8	°C/W	Junction-to-ambient thermal resistance
θ_{JA} (1 m/s airflow)	35.5	°C/W	Junction-to-ambient thermal resistance
θ_{JA} (2 m/s airflow)	34.1	°C/W	Junction-to-ambient thermal resistance
ψ_{JT} (0 m/s airflow)	0.17	°C/W	Junction-to-top center of case thermal resistance
ψ_{JT} (1 m/s airflow)	0.19	°C/W	Junction-to-top center of case thermal resistance

Table 37. Thermal Resistances *(continued)*

ψ_{JT} (2 m/s airflow)	0.24	°C/W	Junction-to-top center of case thermal resistance
θ_{JB}	28.6	°C/W	Junction-to-board thermal resistance
θ_{JC}	13.6	°C/W	Junction-to-case thermal resistance

24.4 Package Thermal Specifications - 100 TFBGA

Table 38. Thermal Specifications - 100-Ball TFBGA 9 × 9mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A	0		70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		13.6		°C/W	Junction-to-case thermal resistance
Ψ_{JT}		0.17		°C/W	Junction-to-top center of case thermal resistance

24.5 Current and Power Consumption Estimates

Power supply current and power consumption information is provided below for PCB design targets.

VDDIO at 3.3 V, SerDes-Cat-5, FD,1518-byte random data packet,100% utilization, SCLK disabled, SFP mode off, regulator off

Table 39. VDDIO at 3.3 V, SerDes-Cat-5, SCLK Disabled

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	109	111	114	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	295	330	367	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	31	36	39	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	731.64	841.8	968.76	mW	Power consumption

VDDIO at 3.3 V, SGMII-Cat-5 (1000 Mbps), FD, 1518-byte random data packet,100% utilization, SCLK disabled, SFP mode off, regulator off

Table 40. VDDIO at 3.3 V, SGMII-Cat-5 (1000 Mbps), SCLK Disabled

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	109	111	114	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	295	330	367	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	31	36	39	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	731.64	841.8	968.76	mW	Power consumption

VDDIO at 3.3 V, SGMII-Cat-5 (100 Mbps), FD, 1518-byte random data packet, 100% utilization, SCLK disabled, SFP mode off, regulator off

Table 41. VDDIO at 3.3 V, SGMII-Cat-5 (100 Mbps), SCLK Disabled

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	89	91	94	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	110	122	135	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	22	24	28	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	450.48	511.8	590.58	mW	Power consumption

VDDIO at 3.3 V, SGMII-Cat-5 (10 Mbps), FD, 1518-byte random data packet, 100% utilization, SCLK disabled, SFP mode off, regulator off

Table 42. VDDIO at 3.3 V, SGMII-Cat-5 (10 Mbps), SCLK Disabled

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	146	151	155	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	53	56	61	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	22	25	28	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	556.5	631.8	716.94	mW	Power consumption

VDDIO at 3.3 V SerDes-Cat-5, FD,1518-byte random data packet,100% utilization, SCLK enabled, SFP mode off, regulator off

Table 43. VDDIO at 3.3 V SerDes-Cat-5, SCLK Enabled

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	109	111	114	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	305	340	379	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	31	36	39	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	743.04	853.8	983.88	mW	Power consumption

VDDIO at 3.3 V, SerDes-Cat-5, FD,1518-byte random data packet,100% utilization, SCLK disabled, SFP mode on, regulator off

Table 44. VDDIO at 3.3 V SerDes-Cat-5, SFP Mode On

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	109	111	114	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	0.5	0.5	0.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
I_{VDD12}	258	275	283	mA	Digital 1.2 V core power supply current into VDD12 pins
I_{VDD12A}	31	36	39	mA	Analog 1.2 V core power supply current into VDD12A pins
P_D	689.46	775.80	862.92	mW	Power consumption

VDDIO @ 3.3V, SGMII-100BASE-FX, FDX, 1518 Byte Random data packet, 100% Utilization, SFP Mode Off

Table 45. VDDIO at 3.3V SGMII-100BASE-FX, SFP Mode Off

Symbol	Min	Typ	Max	Unit	Description
I_{VDD12} + I_{VDD12A}		145		mA	Power supply current into VDD12 and VDD12A pins
I_{VDD33A}		96		mA	Analog 3.3V power supply current into VDD33A pins
$I_{VDDIOMAC}$ + $I_{VDDIOCTRL}$ + $I_{VDDIOMICRO}$		19		mA	Digital I/O supply current into VDDIOMAC, VDDIOCTRL, and VDDIOMICRO pins
P_D		554		mW	Power dissipation

VDDIO at 3.3 V, SerDes-Cat-5, FD,1518-byte random data packet, 100% utilization, SCLK disabled, SFP mode on, regulator on

Table 46. VDDIO at 3.3 V SerDes-Cat-5, SFP Mode On, Regulator On

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33A}	109	111	114	mA	Analog 3.3 V power supply current into VDD33A pins
I_{VDDREG}	149.5	139.5	129.5	mA	1.2 V regulator power supply current into the VDDREG pins
I_{VDDIO}	8	8	10	mA	Digital I/O supply current into VDDIO

Table 46. VDDIO at 3.3 V SerDes-Cat-5, SFP Mode On, Regulator On *(continued)*

Symbol	Min	Typ	Max	Unit	Description
$I_{VDDIOMICRO}$	2	2	2	mA	Digital I/O supply current into VDDIOMICRO
$I_{VDDIOCTRL}$	0.5	0.5	0.5	mA	Digital I/O supply current into VDDIOCTRL
P_D	807.0	861.3	921.6	mW	Power consumption

25 DC SPECIFICATIONS

25.1 Digital Pins (VDDIO = 3.3 V)

The following specifications are valid only when $T_{Ambient}$ = 25 °C, VDDIO = 3.3 V, VDD12 = 1.2 V, VDD33A = 3.3 V, VSS = 0 V.

Table 47. Digital Pins Specifications (VDDIO = 3.3 V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.4		VDDIO	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.5 mA
V_{OL}	GND		0.4	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.5 mA
V_{IH}	2.0			V	Input high voltage.
V_{IL}			0.8	V	Input low voltage.
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.

25.2 Digital Pins (VDDIO = 2.5 V)

The following specifications are valid only when $T_{Ambient}$ = 25 °C, VDDIO = 2.5 V, VDD12 = 1.2 V, VDD33A = 3.3 V, VSS = 0 V.

Table 48. Digital Pins Specifications (VDDIO = 2.5 V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.0		VDDIO	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.0 mA
V_{OL}	GND		0.4	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.0 mA
V_{IH}	1.7			V	Input high voltage. VDDIO = MIN
V_{IL}			0.7	V	Input low voltage. VDDIO = MIN
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.

25.3 LED Output Pins (LED[2:0])

The following specifications are valid over a voltage range of 2.3 V to 1.3 V applied to the LED[2:0] pins.[1]

Table 49. LED Output Pins Specification

Symbol	Max	Recommended[1]	Unit	Parameter Description
$I_{sinking}$	40	8	mA	Current sinking capability of the LED drivers

[1] This recommendation is purely from a power savings view point.

[1]It is assumed that a typical LED will have a forward voltage drop of between 1v and 2v, thereby asserting a 1.3v (3.3v-2v) to 2.3v (3.3v-1v) signal across the LED.

26 CLOCKING SPECIFICATIONS

26.1 Reference Clock Option

The following component specifications should be used to select a clock reference for use with the VSC8221. For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs*, available from the Vitesse Web site.

Table 50. Reference Clock Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$F_{TOL-25MHZ}$	-100 ppm	25	+100 ppm	MHz	Total frequency offset tolerance (25 MHz clock option), including, initial offset, stability over temperature.
T_{R1}, T_{F1}			4	ns	Rise and fall time (20% to 80%), 25 MHz clock option.
T_{R2}, T_{F2}			0.8	ns	Rise and fall time (20% to 80%), 125 MHz clock option.
DUTY	45		55	%	Duty cycle (25 MHz and 125 MHz clock options).

26.2 Crystal Option

The following component specifications should be used to select a crystal for use with the VSC8221. For more information about clocking and frequency offset tolerance specifications when jumbo packet support is required, see the application note *Using Jumbo Packets with SimpliPHYs*, available from the Vitesse Web site.

Table 51. Crystal Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{REF}		25		MHz	Fundamental mode, AT-cut type, parallel resonant crystal reference frequency.
$F_{TOL(TOTAL)}$	-50		+50	ppm	Fundamental mode, AT-cut type, parallel resonant crystal total frequency offset, including, initial offset, stability over temperature, aging and capacitive loading.
C_L	18		20	pF	Crystal parallel load capacitance.
C_{L-EXT}		30		pF	Crystal external load capacitors to GND.[1]
ESR		10	30	Ω	Equivalent series resistance of crystal.
P_D			0.5	mW	Crystal oscillator drive level.

[1] These values can depend on board parasitics.

27 SERDES SPECIFICATIONS

All specifications valid for $T_{Ambient}$ = 0°C to 70°C.

Table 52. SerDes Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_lock		500		uS	Frequency Lock Time
Vidiff	100		2400	mV	Peak to peak differential voltage (TDP-TDN) terminated with a 100 Ω (differential) Load
Vodiff[1]	350	1200	1400	mV	Peak to peak differential voltage (RDP-RDN), 100 Ω (differential) termination in the module, recommended voltage range is 500 mV to 1200 mV
Vicm	0.437 x VDD12	.45 x VDD12	0.464 x VDD12	V	Input common mode voltage
Vocm	0.4 x VDD12	.45 x VDD12	0.5 x VDD12	V	Output common mode voltage
Tr_HS / Tf_HS			300	ps	20%-80% Transition time. Trise / Tfall of high speed output driver.
RJ		18		ps RMS	Random jitter (1 sigma) as per 802.3 standard. random jitter component at RDP, RDN in serial MAC to CAT5 media category of PHY operating modes.
DJ		38		ps pk-pk	With a K28.5+/K28.5- Pattern. Deterministic jitter at RDP, RDN in serial MAC to CAT5 media category of PHY operating modes.
SerDes Data Rate	1249.375	1250	1250.625	Mbps	SerDes data rate. (+/- 500 ppm)

[1] Vodiff is controlled by Extended MII Register 17E.4:2. The default output swing is 1200mV. For more information, see Section 23.3.2 on page 98.

28 System Timing Specifications

28.1 JTAG Timing

The following specifications are valid only when the I/O power supply (VDDIOCTRL) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 53. JTAG Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK\text{-}Period}$	100			ns	TCK period.
$T_{TCK\text{-}High}$	45			ns	TCK minimum pulse width high.
$T_{TCK\text{-}Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS\text{-}Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS\text{-}Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO\text{-}Delay}$			15	ns	TDO delay from TCK.

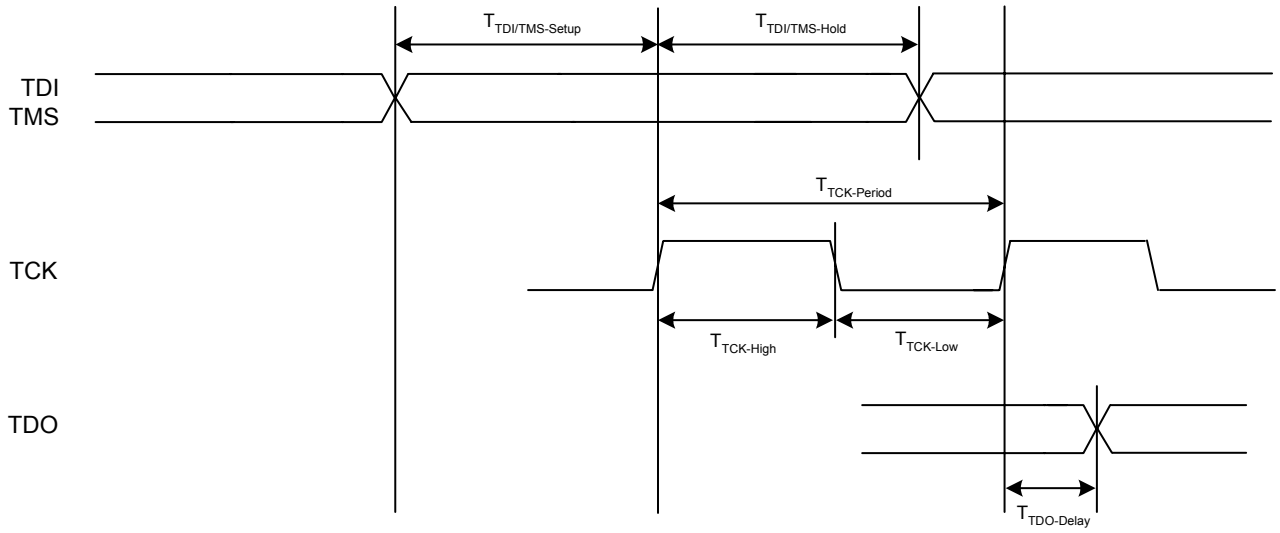


Figure 24. JTAG Interface AC Timing

28.2 SMI Timing

The following specifications are valid only when the I/O power supply (VDDIOMICRO) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 54. SMI Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{MDC}	0	2.5	12.5	MHz	MDC clock frequency.
$T_{MDC\text{-}High}$	20	50		ns	MDC clock pulse width high.
$T_{MDC\text{-}Low}$	20	50		ns	MDC clock pulse width low.
$T_{MDIO\text{-}Setup}$	10			ns	MDIO to MDC setup time when sourced by the station manager.
$T_{MDIO\text{-}Hold}$	10			ns	MDIO to MDC hold time when sourced by the station manager.
$T_{MDIO\text{-}Delay}$		10	300	ns	MDC to MDIO delay time from VSC8221. Delay depends on the value of external pull-up resistor on MDIO pin.

Note: A 4.7k to 10k pullup is recommended on the $\overline{\text{MDINT}}$.

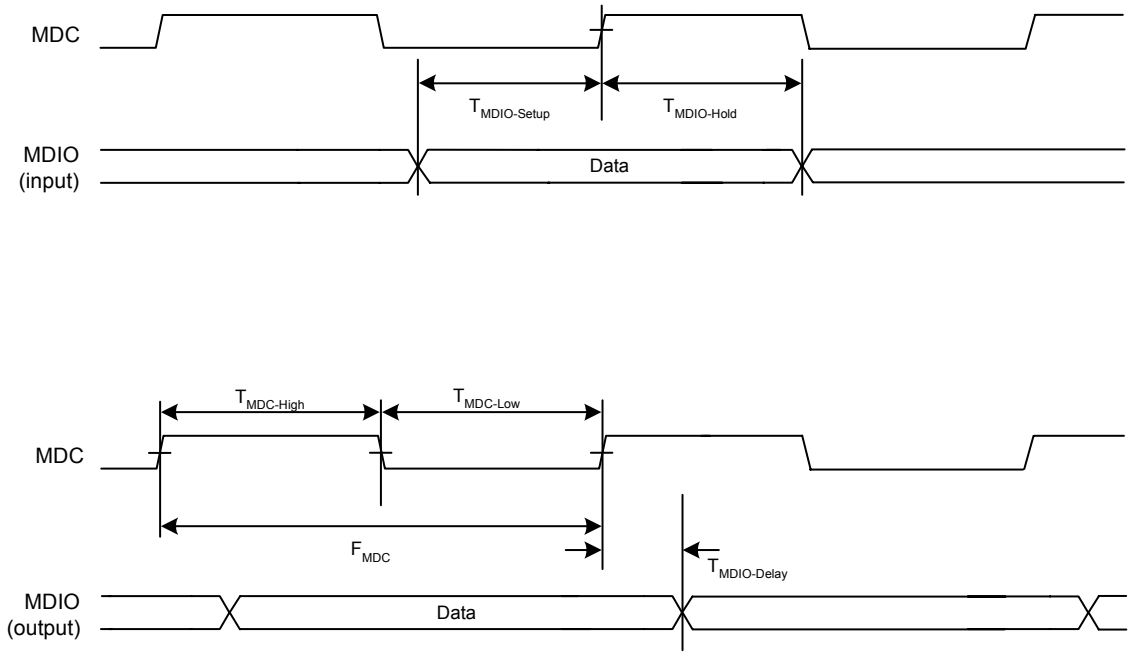


Figure 25. SMI AC Timing

28.3 $\overline{\text{MDINT}}$ Timing

The following specifications are valid only when the I/O power supply (VDDIOMICRO) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 55. $\overline{\text{MDINT}}$ Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_F			110	ns	$\overline{\text{MDINT}}$ fall time, assuming a 2.2 kΩ external pull-up resistor and a 50 pF total capacitive load.

28.4 Serial LED_CLK and LED_DATA Timing

The following specifications are valid only when the I/O power supply (VDD33A) is at 3.3V, ±5%.

Table 56. Serial LED_CLK and LED_DATA Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{LED_CLK}		1		µs	LED_CLK output period.
$T_{LED_CLK\text{-}Pause}$		25		ms	LED_CLK pause between LED bit sequence repeat (un-preambled mode).
$T_{LED_DATA\text{-}Delay}$		0.5		µs	LED_DATA propagation delay from rising edge of LED_CLK.

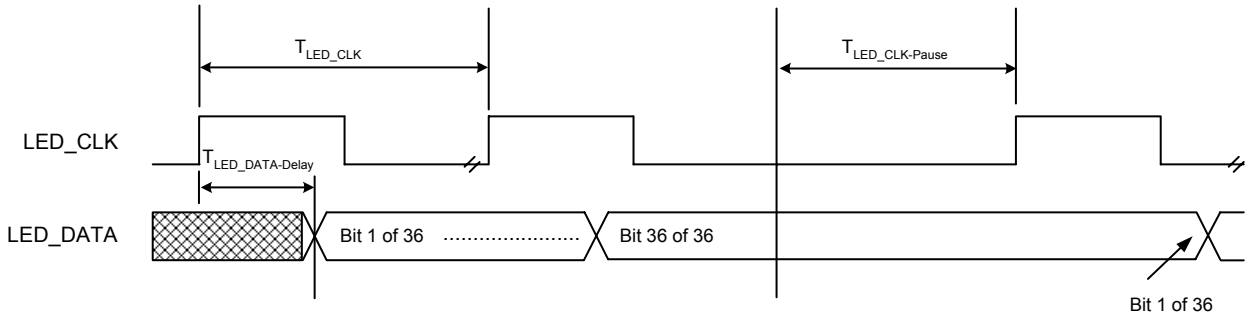


Figure 26. LED_CLK and LED_DATA Output AC Timing

28.5 REFCLK Timing

The following specifications are valid only when the VDD33A is at 3.3 V, ±5%.

Table 57. REFCLK Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		ns	Reference clock period, PLLMODE = 0 (25 MHz reference).
$T_{REFCLK125}$		8		ns	Reference clock period, PLLMODE = 1 (125 MHz reference).
$F_{STABILITY}$			100	ppm	Reference clock frequency stability (0 °C to 70 °C).
T_{DUTY}	40	50	60	%	REFCLK duty cycle in both 25 MHz and 125 MHz modes.
$J_{REFCLK25}$, $J_{REFCLK125}$			300	ps	Total jitter of 25 MHz or 125 MHz reference clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25 MHz mode (20% to 80%).
$t_{R/F\ (REFCLK125)}$			1	ns	Reference clock rise time, 125 MHz mode (20% to 80%).

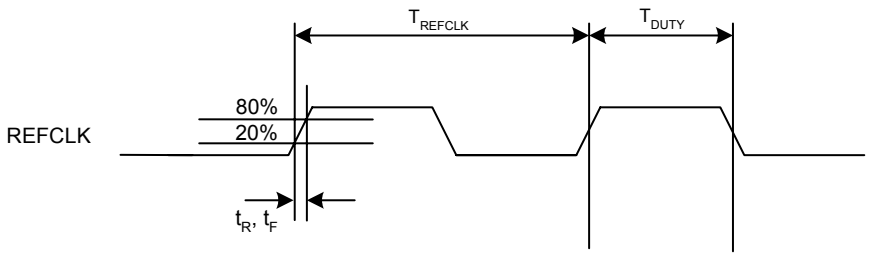


Figure 27. REFCLK AC Timing

28.6 CLKOUT and CLKOUTMICRO Timing

The following specifications are valid only when the I/O power supply (VDDIO for CLKOUT and VDDIOMICRO for CLKOUTMICRO) is at either 3.3 V ±5%, or 2.5 V ±5%.

.

Table 58. CLKOUT and CLKOUTMICRO Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{CLKOUT}		8		ns	Clock period.
$T_{CLKOUTMICRO}$		250 8		ns	Clock period. Either: 4 MHz or 125 MHz.
$F_{STABILITY}$			100	ppm	Clock frequency stability (0 °C to 70 °C).
T_{DUTY}	40	50	60	%	Clock duty cycle.
J_{CLK125}			300	ps	Total jitter of clock (peak-to-peak).
$t_{R/F\ (CLK125)}$			1	ns	Clock rise time (20% to 80%).

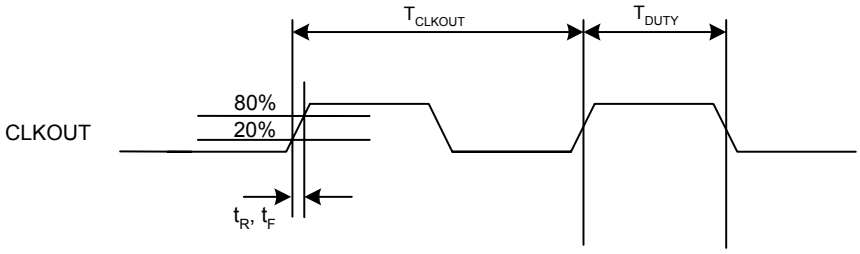


Figure 28. CLKOUT AC Timing

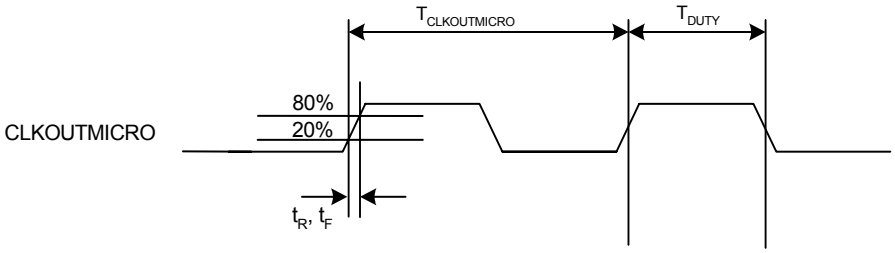


Figure 29. CLKOUTMICRO AC Timing

28.7 Reset Timing

The following specifications are valid only when the I/O power supply (VDDIOmicro) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 59. $\overline{\text{RESET}}$ AC Timing Specification

Symbol	Min	Typ	Max	Unit	Description	Conditions
T_{RESET}	100			ns	Reset assertion time	
T_{READY}		13	20	ms	Reset to SMI active time	If EEPROM is present, an additional 100ms is required

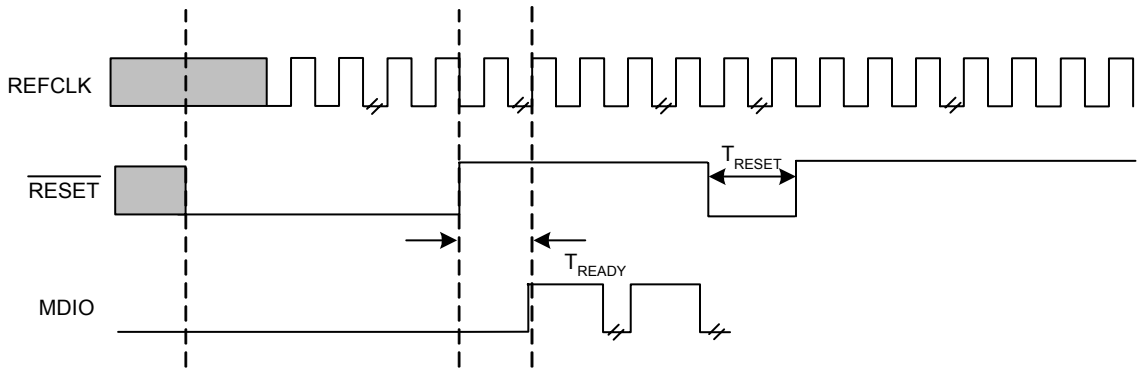


Figure 30. $\overline{\text{RESET}}$ AC Timing

29 PACKAGING SPECIFICATIONS

29.1 100-Ball 9 × 9mm TFBGA Mechanical Specification

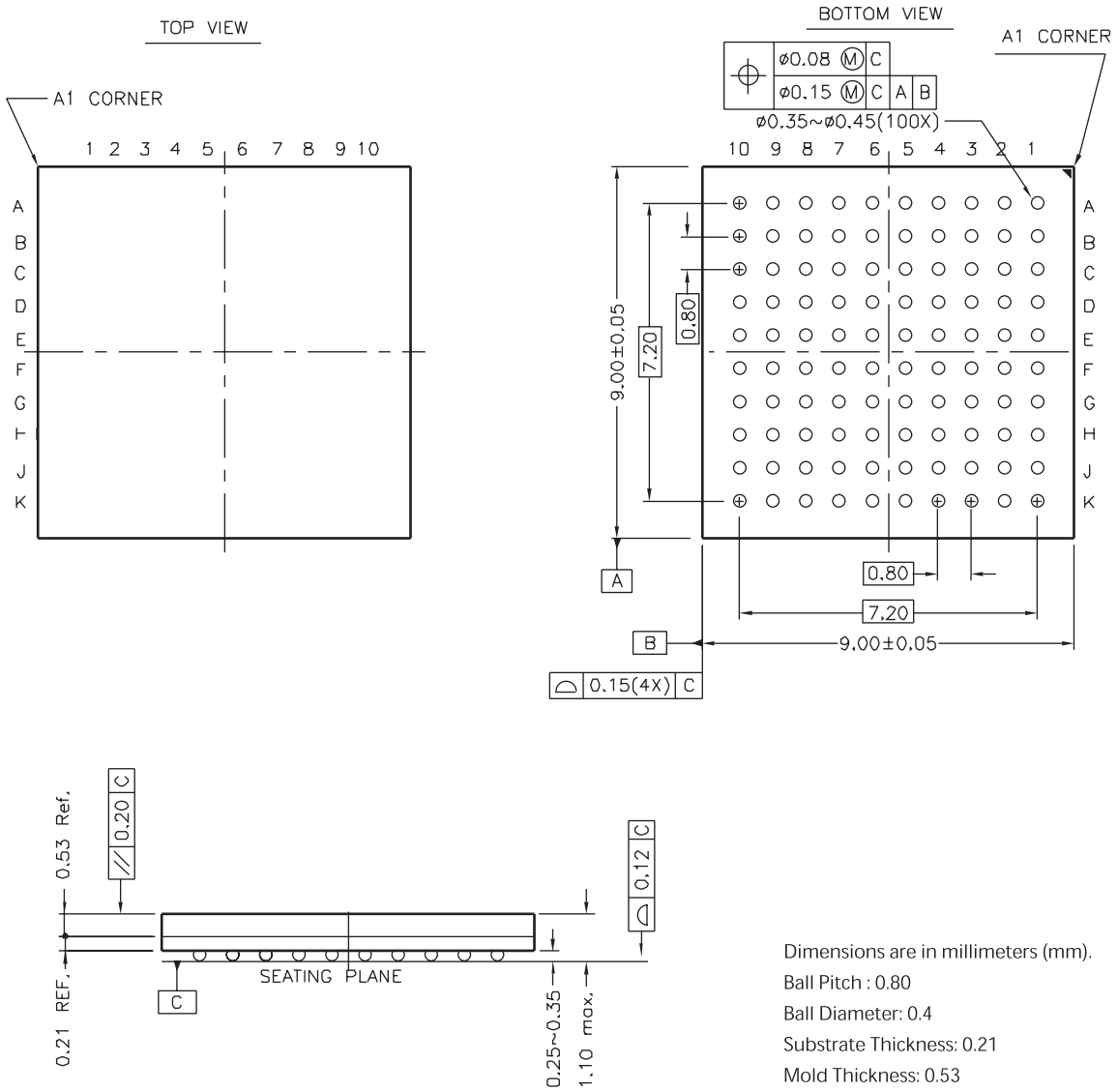


Figure 31. 100-Ball 9 × 9mm TFBGA Mechanical Specification

29.2 Package Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with JEDEC standard IPC/JEDEC J-STD-020B. All Vitesse products are rated moisture sensitivity level 3 or better unless specified otherwise. For more information, see the JEDEC standard.

30 Ordering Information

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the JEDEC standard PC/JEDEC J-STD-020. For more information, see the JEDEC standard.

30.1 Devices

Table 60. Part Number for the VSC8221

Part Number	Package Type	Description
VSC8221HH	100 TFBGA 0.8mm ball pitch 9mm x 9mm body	Single port, low power, triple-speed PHY
VSC8221XHH	100 TFBGA 0.8mm ball pitch 9mm x 9mm body	Lead(Pb)-free, single port, low power, triple-speed PHY

31 DESIGN GUIDELINES

Although copper-based Ethernet physical layer devices (PHY) have been developed from an established IEEE standard, some PHYs available in the marketplace are either non-compliant with the standard or implement non-standard features that cause interoperability issues with the SimpliPHY™ series of gigabit Ethernet PHYs.

31.1 Required PHY Register Write Sequence

Issue: At initialization, a number of internal registers must be changed from their default values.

Description: A series of register writes must be performed after device power-up or reset. These writes can be done using the EEPROM connected to the EEPROM Interface or by the Switch/Station Manager.

Workaround: The required register writes are as follows:

- 2A30h to PHY Register 31
- 0212h to PHY Register 8
- 52B5h to PHY Register 31
- 000Fh to PHY Register 2
- 472Ah to PHY Register 1
- 8FA4h to PHY Register 0
- 2A30h to PHY Register 31
- 0012h to PHY Register 8
- 0000h to PHY Register 31

31.2 Interoperability with Intel 82547EI Gigabit Ethernet MAC+PHY IC

Issue: Due to a non-standard startup-sequence in the Intel 82547EI MAC+PHY IC, the VSC8221 might take multiple attempts to establish link.

Workaround: The following PHY register write can be performed to avoid this issue:

- 0049h to MII Register 18

31.3 SerDes Jitter

Issue: Under worst case conditions, total jitter performance may exceed the IEEE specifications for 1000BASE-X, as noted in the table below.

Impact: In typical applications with robust PCB design practices, however, actual performance is typically better than the figures noted below.

Symbol	Min	Typ	Max	Unit	Parameter Description and Conditions
$J_{(TOTAL, TX)}$			290	ps	Worst case total transmit jitter in media converter applications.
$J_{(TOTAL, RX)}$			400	ps	Worst case total receive jitter tolerance in media converter applications.

Workaround: None.

31.4 SGMII 100BASE-TX Corruption of Packets with Odd Preambles

Description: In SGMII-CAT5 mode and while receiving 100BASE-TX packets with odd preambles, the VSC8221 device's receive rate adaptation block will not properly encode the packet.

The following diagram is an excerpt from Figure 2 of the Cisco SGMII Specification v1.7.

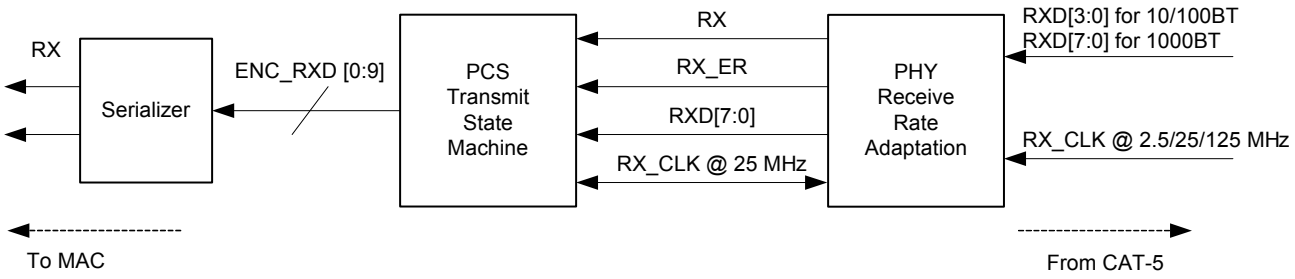


Figure 32. SGMII Rx Path from the PHY to the MAC

Impact: This will cause a normal packet with an odd preamble to become corrupted. The corruption occurs while encoding the SFD. This may cause an otherwise normal packet to be dropped at the MAC.

Example:

Case I : even preamble (correct)

55555Dxyz : encoded as 55, 55, D5, yx …

Case II : odd preamble (incorrect)

5555Dxyz : encoded as 55, 55, xD, zy …

Note no SFD in above

Workaround: There is no workaround at the physical layer of the PHY's packet transmission. If higher layers are being employed on this receive path such as TCP/IP, then a re-transmission request could occur to recover from the loss. This is a problem only when the preamble is corrupted by noise in the CAT5 link or when the link partner PHY is transmitting a non-compliant preamble.

31.5 SGMII 100BASE-TX Corruption of Packets with no ESDs

Description: In SGMII-to-CAT5 mode and while receiving 100BASE-XT packets with no ESD from the CAT5 interface, the 100BASE-TX receive PCS extends the packet by a nibble while asserting RX_ER.

Impact: The rate adaption block subsequently will not transmit this additional nibble and the RX_ER to the MAC. The MAC may then consider this a normal packet.

Workaround: There is no workaround at the PHY's SGMII layer. The likelihood of receiving a packet with no ESD and no CRC error is low. During such an event (if it does occur), the data address and payload are not corrupted. The only item that would be lost is that an RX_ER event occurred to mark the missing ESD during transmission.

For more information, see Figure 32, above.

31.6 Software Reset Time

Description: The VSC8221 device's software reset timing depends on the values of its MII Register 22.9 (Sticky Reset Enable) and its Extended MII Register 21.14 (Re-Read EEPROM on Software Reset).

Table 61. Software Reset Times

Sticky Reset Enable (22.9)	Re-Read EEPROM (21E.14)	Reset Time
1	0	4 microseconds (default)
0	0	300 microseconds
0	1	200 milliseconds
1	1	200 milliseconds

For more information, see Register 0 (00h) – Mode Control Register, page 67, Register 21E (15h) - EEPROM Interface Status and Control Register, page 101, and Register 22 (16h) – Control & Status Register, page 84.

Impact: May cause errors if sufficient delay is not added between software reset and the next register access.

Workaround: System software must ensure that adequate delay is inserted between software reset and the next register address.

31.7 Reducing EMI

Description: In systems that do not use the CLKOUT or the $CLKOUT_{micro}$ outputs, radiated emissions can be reduced by disabling these outputs. Under the default PHY settings, CLKOUT and $CLKOUT_{micro}$ are enabled.

Impact: Reduction of radiated emissions by disabling these unused clock outputs may enable customers to use less expensive system enclosures or shielding methods to reduce system cost.

Workaround: For information about enabling or disabling the CLKOUT output, see Register 18 (12h) – Bypass Control Register, page 81. For information about enabling or disabling the $CLKOUT_{micro}$ output, see Register 17E (11h) - Serdes Control Register, page 98.

31.8 Clause 40 Auto MDI/MDI-X Interoperability Testing

Description: The VSC8221 device's Auto MDI/MDI-X will not pass the UNH IOL's Clause 40 Auto-crossover test suite.

Impact: Although the VSC8221 will not technically pass the entire Auto MDI/MDI-X test suite at the UNH IOL, extensive Auto MDI/MDI-X interoperability testing has been performed in Vitesse's internal interoperability lab, in addition to performing standard interoperability testing at the UNH IOL. Due to the robust Auto MDI/MDI-X implementation in the VSC8221, there are no known interoperability issues with Auto MDI/MDI-X at any speed. Please contact Vitesse for additional interoperability and validation results, including the UNH IOL Test Report.

Workaround: None.

31.9 10BASE-T HDX Issue with IXIA Test Suite

Description: A jam signal generated by an IXIA tester and sent to the VSC8221 in 10BASE-T HDX cannot be seen by a receiving MAC. When a jam signal of 0xFF is generated by an IXIA test suite and transmitted at the start of the packet, the PHY does not report any receive information on its SGMII interface. In SGMII, carrier sense in the MAC is derived from TX_DX, so the MAC is not able to detect a collision.

Impact: The only known situation that could be affected by this issue is if a receive error corrupts the entire preamble. Extensive testing has only shown this error to occur when used with an IXIA tester. This error has not occurred in interoperability testing.

Workaround: None.

31.10 100BASE-FX Initialization Script

The 100BASE-FX initialization script does the following:

- Initializes the copper section of DSP to support the 100BASE-FX mode
- Disables the pair swap option
- Sets 100BASE-X PCS into FX mode
- Forces the PHY into 100Mbps mode

The following script is provided as an attached text file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

```
//--100BASE-FX initialization script for VSC8221.--//

phy_write( phynum(dec), regnum(dec), value(hex) );


phy_write(0, 31, 0x2a30);

phy_write(0,  8, 0x0212);

phy_write(0, 31, 0x52b5);

phy_write(0,  0, 0xa7fa);

phy_write(0,  2, 0x0012);

phy_write(0,  1, 0x3001);

phy_write(0,  0, 0x87fa);

phy_write(0, 31, 0x52b5);

phy_write(0,  0, 0xa240);
```

```
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x0001);
phy_write(0,  0, 0x8240);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa70c);
phy_write(0,  2, 0x00e0);
phy_write(0,  1, 0x000d);
phy_write(0,  0, 0x870c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa70c);
phy_write(0,  2, 0x00e0);
phy_write(0,  1, 0x0000);
phy_write(0,  0, 0x870c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa258);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x2140);
phy_write(0,  0, 0x8258);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa258);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x21c0);
phy_write(0,  0, 0x8258);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25a);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x2940);
phy_write(0,  0, 0x825a);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25a);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x29c0);
phy_write(0,  0, 0x825a);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25c);
phy_write(0,  2, 0x0000);
```

```
phy_write(0,  1, 0x3000);
phy_write(0,  0, 0x825c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25c);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x3000);
phy_write(0,  0, 0x825c);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25e);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x38a0);
phy_write(0,  0, 0x825e);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa25e);
phy_write(0,  2, 0x0000);
phy_write(0,  1, 0x3800);
phy_write(0,  0, 0x825e);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa2);
phy_write(0,  2, 0x0098);
phy_write(0,  1, 0x000);
phy_write(0,  0, 0x8fa2);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa2);
phy_write(0,  2, 0x009c);
phy_write(0,  1, 0x0000);
phy_write(0,  0, 0x8fa2);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa0);
phy_write(0,  2, 0x0013);
phy_write(0,  1, 0x1b00);
phy_write(0,  0, 0x8fa0);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xafa0);
phy_write(0,  2, 0x0013);
phy_write(0,  1, 0x9b00);
```

```
phy_write(0,  0, 0x8fa0);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x0004);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x000c);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x001c);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x52b5);
phy_write(0,  0, 0xa708);
phy_write(0,  2, 0x000e);
phy_write(0,  1, 0x003c);
phy_write(0,  0, 0x8708);
phy_write(0, 31, 0x0000);
phy_write(0, 18, 0x0069);
phy_write(0, 31, 0x0000);
phy_write(0, 18, 0x7069);
phy_write(0, 31, 0x0000);
phy_write(0,  0, 0x2100);
```

32 Product Support

All support documents for the VSC8221 can be accessed on the Vitesse Web site at *www.vitesse.com*. Access to some documents may require filing a non-disclosure agreement with Vitesse.

32.1 Available Documents and Application Notes

- IBIS Model
- OrCAD Symbol
- BSDL File
- Copper SFP PHY Performance Comparison White Paper
- Design and Layout Guidelines application note
- Magnetics Guide
- Using Jumbo Packets with SimpliPHYs application note
- UNH Test Report (requires NDA)
- Designing a Copper SFP using the VSC8221 PHY application note

For additional application notes and information about reference designs using the VSC8221 PHY device, visit the Vitesse Web site at *www.vitesse.com*.

33 Document History and Notices

Revision Number	Date	Comments
0.1.0	Feb 10, 04	First Preliminary Release
0.1.1	May 11, 04	Added VDD12A pin reference. Added Errata Section and added errata no. 6 Updated 'specification' section with VDD12A reference Updated LED ECO
0.1.2	Jun 22, 04	Added 'Connector Loopback section' Added power consumption data. Removed Errata Section, added design guidelines section. Updated MII Register 0.15, 24.0 removed column S.no from table 27.2 (Register 23)
2.0	Aug 18, 04	Updated document style to reflect Vitesse corporate standards. Added two power consumption tables. Added new package diagram. Replaced Cicada silicon revision conventions with the Vitesse silicon revision conventions. A0 (Cicada) is now A (Vitesse). A1 (Cicada) is now C (Vitesse).
2.1	Sep 13, 04	Changed ambient free-air operating temperature and thermal resistance specifications.
4.0	May 02, 05	Removed reference to support of 100BASE-FX (100 Mbps) modules in the Features and Benefits section. Changed description of the System Clock Interface Signals - In XTAL1 crystal oscillator input section. For more information, see Table 5, "System Clock Interface Signals (SCI)," on page 17. Deleted the system schematics that showed power supply connections. Added descriptive information to the section about the device twisted pair interface. For more information, see Section 10, "Twisted Pair Interface" on page 10-29. Added information about the device Auto-MDI/MDI-X in Forced 10/100 Link Speeds. For more information, see Section 10.3, "Auto MDI/MDI-X in Forced 10/100 Link Speeds" on page 10-30. Added information about Forcing the PHY into MDI or MDI-X mode in 10/100/1000 Link Speeds. For more information, see Section 10.4, "Forcing the PHY into MDI or MDI-X mode in 10/100/1000 Link Speeds" on page 10-31. Changed title of SMI pin descriptions table. For more information, see Table 18, "SMI Pin Descriptions - IEEE Mode," on page 38. Added information to the LED Function Assignments table. For more information, see Table 20, "LED Function Assignments," on page 41. Changed the information associated with the device Parallel LED functions. For more information, see Table 21, "Parallel LED Functions," on page 41. Changed information associated with the device identification register. For more information, see Section 14, "Test Mode Interface (JTAG)" on page 14-44. In the Operation in enhanced ActiPHY mode section, changed the illustration showing the enhanced ActiPHY state. For more information, see Figure 16 on page 15-47. In the description of near-end loopback testing, the information about what happens to the signal was changed. For more information, see Section 17.4, "Near-End Loopback" on page 17-52. *(continues)*

Revision Number	Date	Comments
4.0 *(continued)*	May 02, 05	*(continued)* In the description of the connector loopback, the information about connecting the PHY to a loopback connector or loopback cable. For more information, see Section 17.5, "Connector Loopback" on page 17-52. Deleted information about the device SGMII-to-100BASE-FX operation (was page 60 in the previous version of the datasheet). Deleted information about the device's IEEE 802.3 Clause 28 and 37 Remote Fault Indication support (was page 61 in the previous version of the datasheet). Added information to the description of the device mode control register. For more information, see Section 23.2.1, "Register 0 (00h) – Mode Control Register" on page 23-67. Added information to the description of the device mode status register. For more information, see Section 23.2.2, "Register 1 (01h) – Mode Status Register" on page 23-69. Changed information associated with the reset value of the device identification register #2. For more information, see Section 23.2.4, "Register 3 (03h) – PHY Identifier Register #2" on page 23-71. Changed the information associated with certain reset values in the device PHY control register #2. For more information, see Section 23.2.25, "Register 24 (18h) – PHY Control Register #2" on page 23-87. Changed the information associated with the reset value in the device LED control register. For more information, see Section 23.2.28, "Register 27 (1Bh) – LED Control Register" on page 23-92. Changed the information associated with the enhanced ActiPHY mode enable bit in the device auxilliary control and status register. For more information, see Section 23.2.29, "Register 28 (1Ch) – Auxiliary Control and Status Register" on page 23-94. Information on the SIGDET pin direction when the device is operating in serial MAC-to-CAT-5 media and Fiber media modes was changed. For more information, see Section 23.3.4, "Register 19E (13h) - SerDes Control # 2" on page 23-99. The reset value for bits 8 and 4 in the Extended PHY control register #3 were changed. For more information, see Section 23.3.5, "Register 20E (14h) - Extended PHY Control Register #3" on page 23-100. Also changed description of bit 5 in this register. The specification for ESD according to the Machine Model (VESD(MM)) was deleted from the Electrical Specifications section. Information about the ESD sensitivity of the device was added. For more information, see Section 24.1, "Absolute Maximum Ratings" on page 24-107. The device operating temperature specification was changed. For more information, see Section 24.2, "Recommended Operating Conditions" on page 24-107. Added qualifying description to estimates of current and power consumption. For more information, see Section 24.5, "Current and Power Consumption Estimates" on page 24-109. Changed the power consumption specification for the device with VDDIO at 3.3V, in SerDes-to-Cat-5 mode, FD, 1518-byte randmom data packet, 100% utilization; and with SCLK, SFT and regulator off. For more information, see Table 39, "VDDIO at 3.3 V, SerDes-Cat-5, SCLK Disabled," on page 109. Changed the power consumption specification for the device with VDDIO at 3.3V, in SGMII-to-Cat-5 mode (1000 Mbps), FD, 1518-byte randmom data packet, 100% utilization; and with SCLK, SFT and regulator off. For more information, see Table 40, "VDDIO at 3.3 V, SGMII-Cat-5 (1000 Mbps), SCLK Disabled," on page 110. *(continues)*

Revision Number	Date	Comments
4.0 *(continued)*	May 02, 05	*(continued)* Changed the power consumption specification for the device with VDDIO at 3.3V, in SGMII-to-Cat-5 mode (100 Mbps), FD, 1518-byte randmom data packet, 100% utilization; and with SCLK, SFT and regulator off. For more information, see Table 41, "VDDIO at 3.3 V, SGMII-Cat-5 (100 Mbps), SCLK Disabled," on page 110. Changed the power consumption specification for the device with VDDIO at 3.3V, in SGMII-to-Cat-5 mode (10 Mbps), FD, 1518-byte randmom data packet, 100% utilization; and with SCLK, SFT and regulator off. For more information, see Table 42, "VDDIO at 3.3 V, SGMII-Cat-5 (10 Mbps), SCLK Disabled," on page 111. Changed the power consumption specification for the device with VDDIO at 3.3V, in SerDes-to-Cat-5 mode, FD, 1518-byte randmom data packet, 100% utilization; and with SFT and regulator off, SCLK on. For more information, see Table 43, "VDDIO at 3.3 V SerDes-Cat-5, SCLK Enabled," on page 111. Changed the output high voltage specification for the digital pins when VDDIO = 3.3 V. Also changed the specification for the output low voltage. Also changed the specification for the input high voltage. Also changed the specification for the input low voltage. For more information, see Table 47, "Digital Pins Specifications (VDDIO = 3.3 V)," on page 114. Changed the specification for random jitter (RJ) in the SerDes specifications table. For more information, see Table 52, "SerDes Specifications," on page 117. Also changed deterministic jitter specification (DJ) in the same table. Added specifications for the device reset timing. For more information, see Section 28.7, "Reset Timing" on page 24-123. Added information about the moisture sensitivity of the device package. For more information, see Section 29.2, "Package Moisture Sensitivity" on page 25-124. Deleted temperature range information from the device ordering information. Added descriptive information and specifications for the device SerDes jitter. For more information, see Section 31.3, "SerDes Jitter" on page 27-126. Added descriptive information, specifications, illustrations and example cases related to the device's corruption of packets with odd preambles when operating in SGMII 100BASE-TX mode. For more information, see Section 31.4, "SGMII 100BASE-TX Corruption of Packets with Odd Preambles" on page 27-127. Added descriptive information related to the device's corruption of packets with no ESDs when operating in SGMII 100BASE-TX mode. For more information, see Section 31.5, "SGMII 100BASE-TX Corruption of Packets with no ESDs" on page 27-127. Added descriptive information and specifications related to the device's software reset timing. For more information, see Section 31.6, "Software Reset Time" on page 27-128. Added descriptive information related to the reduction of EMI. For more information, see Section 31.7, "Reducing EMI" on page 27-128.

Revision Number	Date	Comments
4.1	December 06	• In the media converter application diagram, the RJ-45 speed was corrected from 10/100/1000BASE-T to 1000BASE-T. • Throughout the datasheet, information was added regarding the 100BASE-FX mode. The following lists the main information: – For information about twisted pair signals in 100BASE-FX mode, see Table 12: “Twisted Pair Interface Signals”. – For information about 100BASE-FX system schematics, see Figure 5: "System Schematic - 100Mbps Fiber Media Implementation". – For information about 100BASE-FX connections and initialization, see Section 10.6: "100Mbps Fiber Support Over Copper Media Interface" and Section 31.10: "100BASE-FX Initialization Script". – For information about 100BASE-FX current consumption, see Table 45: “VDDIO at 3.3V SGMII-100BASE-FX, SFP Mode Off”. • In the listing of JTAG interface instruction codes, the register width given for the instructions EXTEST and SAMPLE/PRELOAD was corrected from 196 bits to 72 bits. • In the reset AC timing diagram, the MDIO signal pulse width was widened to be more accurate relative to the pulse width of the REFCLK signal. For more information about this specification, see Figure 30: "RESET AC Timing". • In the reset AC timing specifications, T_{READY} signal, a condition was added that if EEPROM is present, an additional 100ms is required. For more information about reset AC timing, see Table 59: “RESET AC Timing Specification”.

CORPORATE HEADQUARTERS
Vitesse Semiconductor Corporation
741 Calle Plano
Camarillo, CA 93012
Tel: 1-800-VITESSE • FAX:1-(805) 987-5896

For application support, latest technical literature, and locations of sales offices,
please visit our web site at
www.vitesse.com

Copyright © 2004–2006 by Vitesse Semiconductor Corporation

PRINTED IN THE U.S.A

Vitesse Semiconductor Corporation ("Vitesse") retains the right to make changes to its products or specifications to improve performance, reliability or manufacturability. All information in this document, including descriptions of features, functions, performance, technical specifications and availability, is subject to change without notice at any time. While the information furnished herein is held to be accurate and reliable, no responsibility will be assumed by Vitesse for its use. Furthermore, the information contained herein does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

Vitesse products are not intended for use in life support products where failure of a Vitesse product could reasonably be expected to result in death or personal injury. Anyone using a Vitesse product in such an application without express written consent of an officer of Vitesse does so at their own risk, and agrees to fully indemnify Vitesse for any damages that may result from such use or sale.

Vitesse Semiconductor Corporation is a registered trademark. All other products or service names used in this publication are for identification purposes only, and may be trademarks or registered trademarks of their respective companies. All other trademarks or registered trademarks mentioned herein are the property of their respective holders.